Overview

D21X series is a SOC with high-performance full HD display and intelligent control.

It is based on the RISC-V 64bit CPU architecture, it provides rich peripheral interfaces.

It is integrated with 2D graphic engine and H.264 decode engine.

It is used in industrial field with its high reliability, high security and high openness design standards.

Features

✧ CPU内核

- Signal Core 64位RISC-V CPU
- 600MHz@1.2V
- I/D Cache:32KB+32KB

✧ Memory Subsystem

- 32KB BROM，96KB SRAM
- SIP 512Mb DDR2， 504MHz or 1GbDDR3，672MHz
- Support boot media QSPI NAND、QSPI NOR、EMMC、SD card
- Support mass product with USB，SD card
- Support security boot , firmware protection and spi encryption

✧ Multiple Media Subsystem

- Support PNG decode (up to 4K*4K), JPEG decode(up to 8K*8K)
- Support 2D graphic engine, up to 4094*4096, support fixed angle rotation, color space conversion, scaling, image dithering, alpha blending, different formats overlay, font overlay with alpha grayscale and so on
- Support display accelerate, up to 1080p@60fps, Display output rows/columns up to 4096, support UI and video two layer overlay, and support write back
- Support rich display interface, including RGB888, LVDS up to 1080P, MIPI-DSI up to 1080P, I8080, SPI
- Support CMOS DVP parallel digital interface, with maximum support 1080p@30fps image input, or 5Mpixels for photos, support YUV422 and BT565 formats
- Support 2 digital MIC and 1 analog MIC, 2 PWM audio outputs, 1 I2S/PCM

✧ Peripherals

- Dual 10/100/1000m Ethernet GMAC
- Dual USB port, supporting master and slave switch
- Up to 3 SPI interface
- Up to 2 SD Cards/SDIO
- Up to 8 UART, supporting automatic switching of RS485 transmission and control signals
- Up to 4 TWI interface, compatible with I2C
- Up to 2 CAN 2.0B compatible interface
- One 16bit programmable parallel port bus, can be used to connect FPGA
- 6 sets of GPIOs with a total of 100 independently configurable IOs
- 1 sets of CIR, supporting infrared input and output
- Support for 4-wire RTP

✧ RTC Subsystem

- Built in oscillator, external 32768Hz crystal required

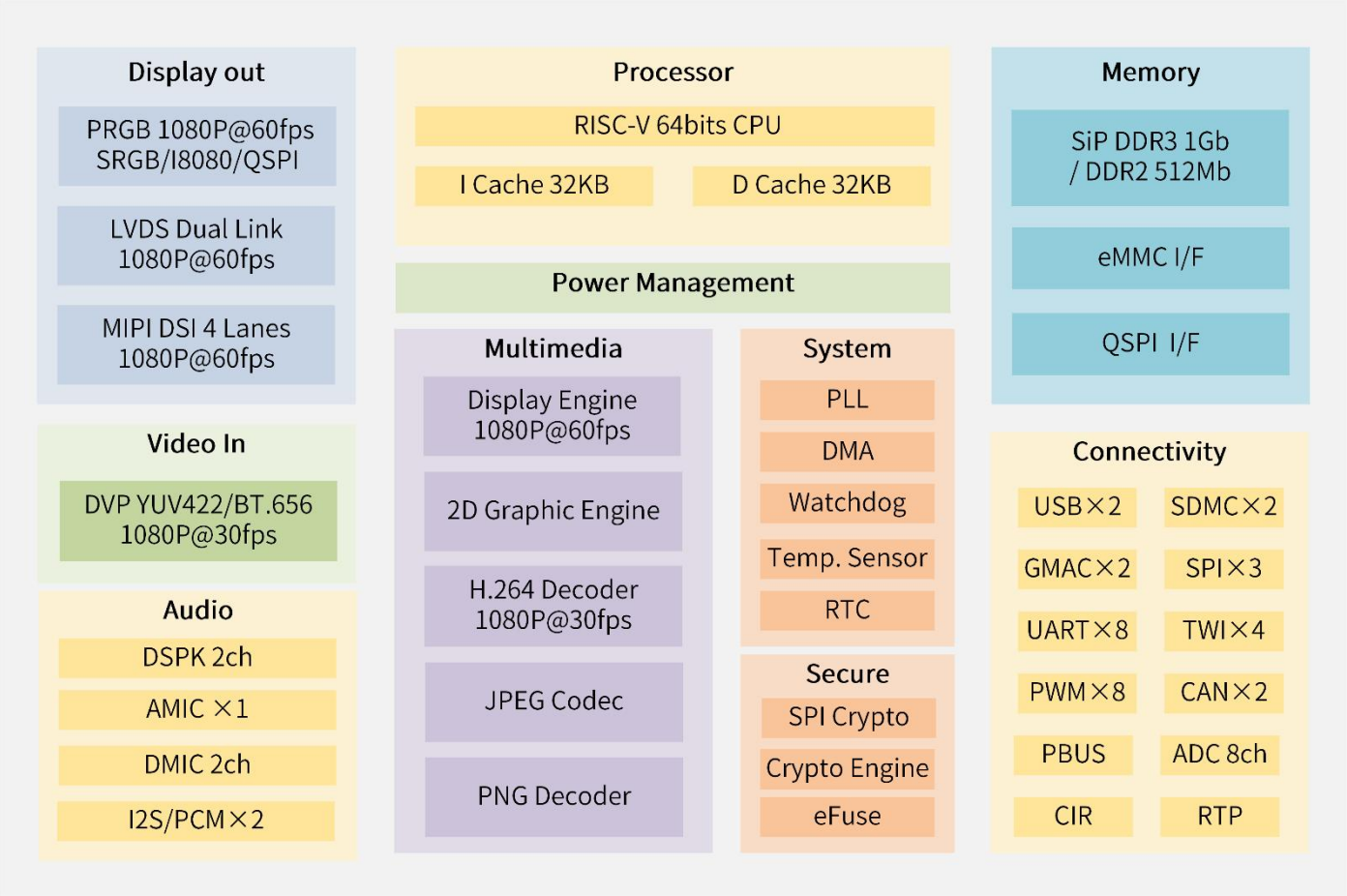
- Built in 128bit universal read/write register
- Built-in 32bit timer
- Support Alarm function, use IO to output Alarm signal
- Built in software calibration function
- Minimum sleep power consumption<2uA
- Built in automatic switch cell for power supply and battery

✧ Package

- QFN88（10*10mm 0.4mm pitch）
- QFN100（12*12mm 0.4mm pitch）
- QFN128（12.3*12.3mm 0.35mm pitch）
- SIP 512Mb DDR2 or 1Gb DDR3
- Tj -40~125℃

✧ Software

- Deep customized based on Buildroot2
- Support both Linux and RTO
- Linux-5.10 and uboot-2021.10
- RTOS supports Baremetal，Freertos and Rt-thread
- QT 4.8.7 + LVGL 8.3 + GStreamer 1.20.3
- 5 minutes compile complete
- 1.9 seconds system startup
- System memory use <8MB



D21X Architecure