D21x Datasheet

Version 1.4

Revision Date: 2024-10-17

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Revision History

Version	Section	Description
V1.3	–	Aligned styles.
	Functional Features	Changed the descriptions.
	Product Information	Modified the product comparison table.
		• Modified the minimum value for VCC330_IO and VCC33_IO1 in the operating conditions. • Updated the typical operating current in RTC Power Supply. • Modified the descriptions for reset sources.
	Package Information	• Updated pin attributes.
V1.4	Power–on/Power–off Sequence and Reset	Added the following description: • The rising edge working at 3.3V shall be detected after 150 us. • The RTC_VCOIN (Real–Time Clock Voltage Input) requires an RC–delayed power–up circuit.

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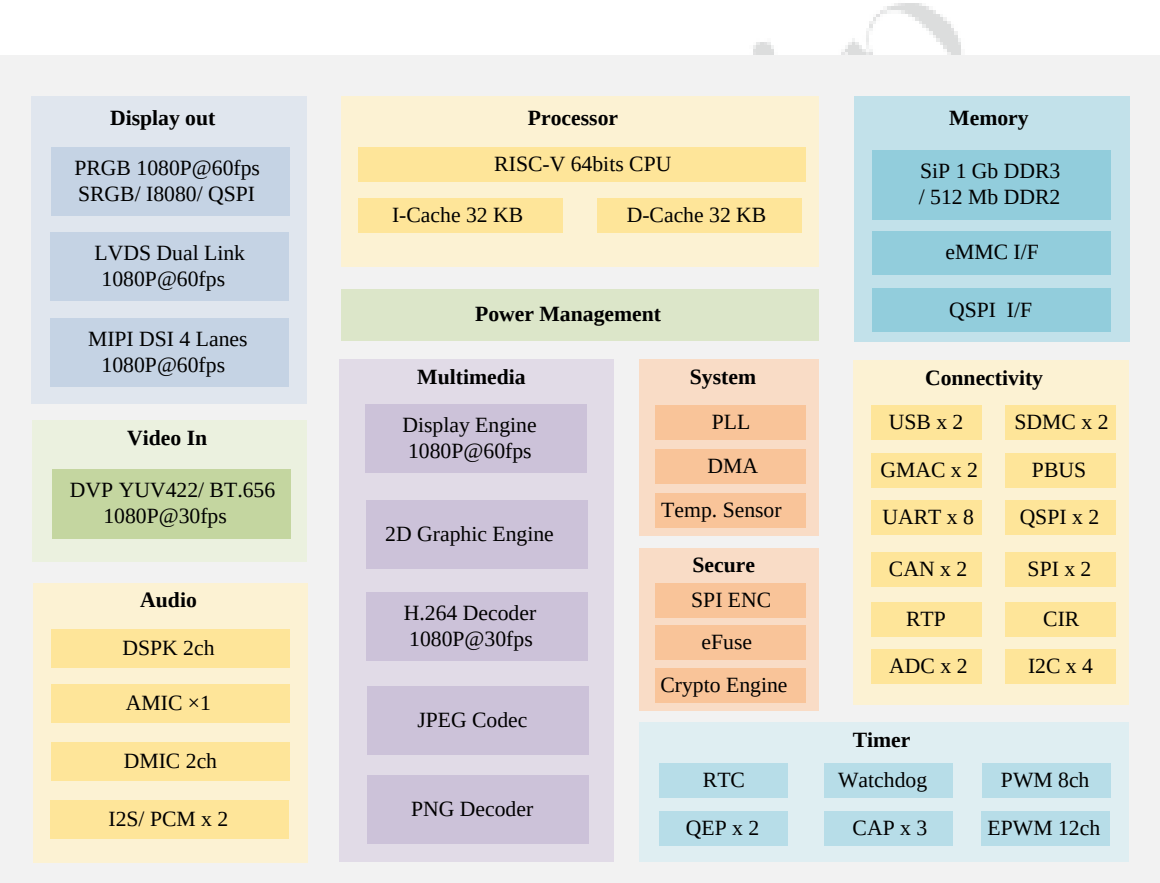
1. Introduction

D21x is a high-performance SoC with full HD display and intelligent control. It is integrated with a domestically independent 64-bit high-computing-power RISC-V core and an internal 16-bit DDR controller.D21x provides rich peripheral interfaces for extended connectivity. The 2D image acceleration engine and H.264 decoding engine are also integrated on the D21x SoC to provide all kinds of interaction scenarios and multimedia interactive experience. D21x is designed for pan-industrial applications with high reliability, high security, and highly open design standards.



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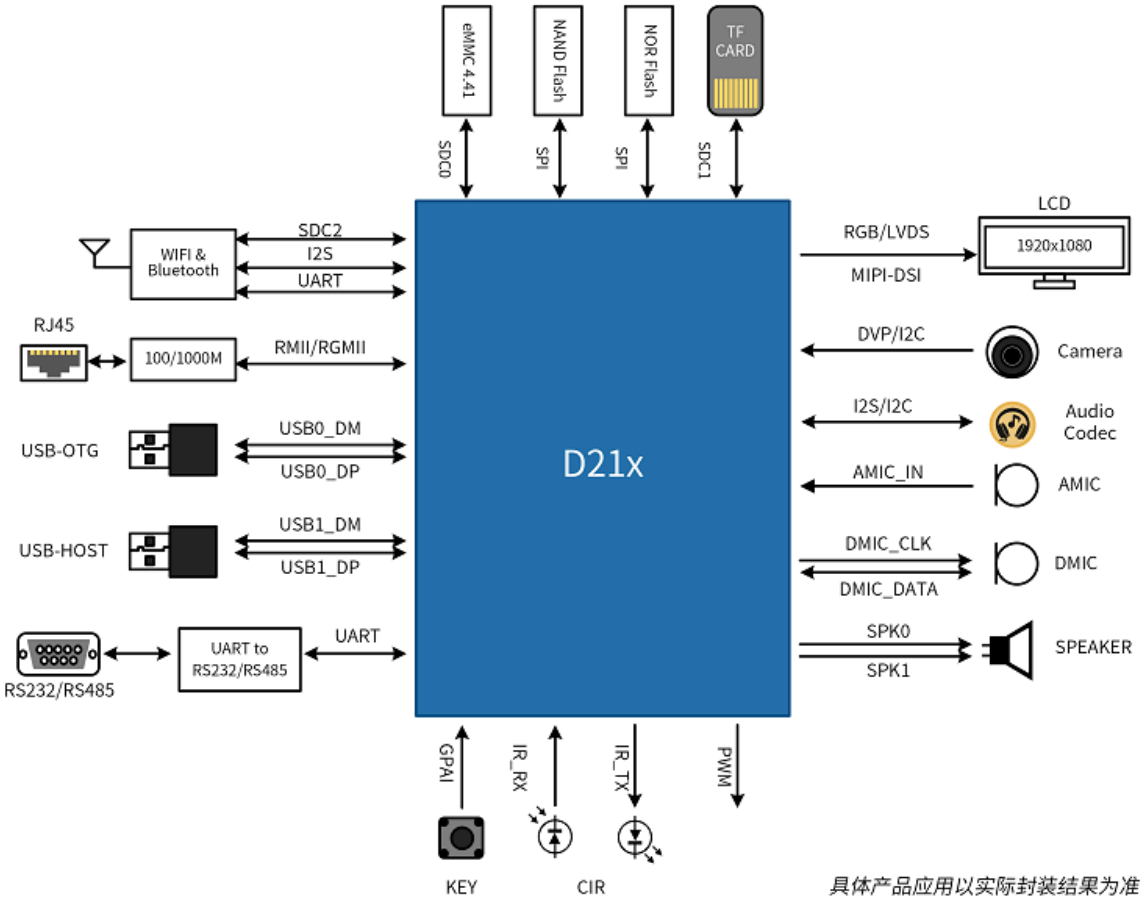

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2. Functional Features

CPU Core

- T-Head C906 processor, RV64IMAFDC instruction extension, 600MHz @ 1.2V
- 32-KB L1 instruction cache and 32 KB L1 data cache
- Single/double-precision floating-point unit (FPU)
- Sv39 virtual address system and physical memory protection (PMP)
- Standard CLINT and PLIC interrupt controllers

Boot

- Default boot sequence: SD Card (SDMC1) → NAND (QSPI0) → NOR (QSPI0) → eMMC (SDMC0)
- Default boot device configuration available by burning eFuse
- Upgrade by burning USB and SD Card (SDMC1) forced upgrade supported

System Safety

- Secure boot by digital signatures
- Crypto Engine (CE) with support for AES/ TDES/ RSA and SHA/ HMAC
- SPI NAND/SPI NOR decode algorithms for SPI ENC
- The built-in eFuse one-time programmable memory has 2048 bits, of which 512 bits are available for customer customization. It has an independent CHIPID and supports CE security key functions such as SSK/ HUK/PNK/PSK0/PSK1/PSK2/PSK3. It also supports setting read and write prohibitions.
- Embedded 256-bit TRNG

On-chip Memory

- 32 -KB BROM
- 96 KB SRAM
- DRAM with two options:
  - 512 Mb DDR2 with a 16-bit bus width and a maximum frequency of 504 MHz.
  - 1Gb DDR3 with a 16-bit bus width and a maximum frequency of 672 MHz
- DRAM clock with spread spectrum function.

Memory Interfaces

- SPI NAND Flash / SPI NOR Flash for QSPI
  - Standard, dual SPI and quad SPI supported
  - Up to 100-MHz SDR for IO
- Three sets of eMMC 4.41/ SD 2.0/ SDIO 2.0
  - 8-bit or 4-bit SDR25/ SDR50/ DDR50 data transfer for eMMC
  - SDR25/ SDR50 supported for SD cards
  - Up to 50-MHz of DDR for IO with 3.3 V voltage support only

Graph Engine

- Disply Engine (DE)
  - One UI layer and one VI layer with the highest performance of 1080P@60fps
  - 1/31.999x ~ 32x scaling support for VI layer
  - Dither function
- Graph Engine
  - 2D image acceleration, with a performance of up to 1080P@60fps
  - Horizontal and vertical flip support with 90/180/270-degree rotation angles
  - Rotation at any angle and scan order support for RGB graphs
  - 1/16x ~ 16x scaling scope support and 6x4-tap 16-phase filtering algorithm
- VE CODEC
  - H.264/AVC decoder with the highest performance of 1080P@30fps
  - MJEPG decoder with the highest performance of 1080P@60fps
  - PNG decoder, with the highest performance of 1080P@15fps
  - JPEG decoder, with the highest performance of 1080P@60fps

Display Interfaces

- 24-bit parallel port RGB, with the highest performance of 1080P@60fps
- Single Link or dual-link LVDS with up to 700 Mbps of IO rate and 1080P@60fps of performance

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- 1/ 2/ 4–Lne MIPI DSI with up to 1 Gbps of IO rate and 1080P@60fps of performance
- SRGB/I8080/QSPI interfaces with up to 200 Mbps of IO rate
- 8–bit DVP with up to 150 MHz of IO rate and 1080P@30fps of performance
- Spread spectrum

Audio Interface

- One Audio ADC (AMIC)
- One DMIC interface with left and right channel input
- Two I2S interface with input/ output and I2S/ PCM/ TDM modes
- Two digital PWM outpus (DSPK) with support for two single–ended L/R channels and one differential mono channel

General Interface

- Two USB2.0 ports: USB0 can be configured as DEVICE/ HOST, and USB1 can be configured as HOST
- Two GMAC with selectable 100M RMII/1000M RGMII interfaces and IEEE1588 protocol support
- Two QSPI interfaces for standard, dual SPI and quad SPI, configurable as Master
- Two SPI interfaces for standard SPI, configurable as Master
- Eight or UART ports, supporting 2–wire/ 3–wire/ 4–wire interfaces, compatible with the industrial standard 16550, with a maximum baud rate of 5 Mbps.
- Four I2C interfaces, supporting 7–bit and 10–bit addressing, with a maximum data transfer rate of 400 Kb/s.
- Two CAN modules with support for CAN2.0A and CAN2.0, and up to 1 Mbps of programmable comminicatable speed
- One CIR that supports infrared input and output
- One PBUS with support of 16–bit 100–MHz clock for read and 100 MB/s of write access to the address space of external devices
- Six groups of GPIO, with a total of up to 100 IO ports that are individually configurable:
  - Resistor options: no pullup, pullup 33KΩ, pulldown 33KΩ
  - Eight output driver levels available
  - Two–level dithering and interrupts
  - Bit operation

Timer

- GTC Generic Timers
  - 52–bit timer for system heartbeat clock with over 35 years of clocking cycle
  - Pause or Resume timer configurable in debug mode
- WDOG
  - Interrupt and reset mode with configurable timeout period from 1ms to 37 hours
  - Pause or Resume timer configurable in debug mode
  - Firmware write protection
- Real Time Clock (RTC)
  - Unit in seconds and time span of 100 years with support of alarm settings
  - Support for an external 32.768–KHz oscillator for digital calibration within the range of ± 975 ppm
  - Independent standby power supply input pin for built–in power switch
  - 128–bit register reserved for system data backup suck as key protected data during power down
  - Less than 3.3 uA of RTC typical operating current
- PWM
  - Built–in 16–bit counter with four timers
  - Support for up to eight independent PWM channels or four complementary PWM channels
- EPWM
  - Built–in 16–bit PWM counter, supporting six timers.
  - Up to 12 independent PWM channels or six complementary PWM channels
  - Support for ADC samling triggered by firmware
- CAP

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- Built–in 32–bit CAP counter with three timers
- Up to three–channel input signal captures or three simple PWM signal outputs.
- Continuous capture or single capture mode available

- QEP
  - Up to two QEP signal resolutions
  - Built–in 32–bit positioning counter
  - AB orthogonal signal resolution.
  - CW/CCW signal resolution.
  - CLK/ DIR signal resolution.
  - Built–in 32–bit watchdog timer

Analog

- Built–in 12 –channel 12–bit PSADC, with a maximum sampling rate of 1 Msps.
- Built–in 8–channel 12–bit GPADC, with a maximum sampling rate of 1 Msps.
- Integrated resistive touch pannel (RTP)

Clock and Power Management

- Five built–in PLLs in CMU:
  - PLL_INT0 for CPU only
  - PLL_INT1 for BUS, internal modules, and low speed interface units
  - PLL_FRA0 for memory interfaces with the spread spectrum feature
  - PLL_FRA1 for audio interfaces with support for fractional–N feature
  - PLL_FRA2 for display output modules with the spread spectrum feature
- Three built–in LDO modules for SYSCFG:
  - LDO30 (3.0 V 100 mA), for power supply of system reset boot and Audio ADC
  - LDO25 (2.5 V 50 mA), for power supply of DDR analog system and eFuse modules
  - LDO1x (1.8/ 1.5 V 500 mA) with configurable power outputs
- Embedded THS with support for high and low temperature interrupt alarms

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3. Product Information

Table 3–1 Product

Model	Feature	Package	Temperature (Tj)
D211BBV	64 MB DDR2	QFN88, 10x10mm, 0.4mm	–20 to +105° C
D211BBX	64 MB DDR2	QFN88, 10x10mm, 0.4mm	–40 to +125° C
D211BCV	128 MB DDR3	QFN88, 10x10mm, 0.4mm	–20 to +105° C
D211BCX	128 MB DDR3	QFN88, 10x10mm, 0.4mm	–40 to +125° C
D211DBV	64 MB DDR2	QFN100, 12x12 mm, 0.4 mm	–20 to +105° C
D211DBX	64 MB DDR2	QFN100, 12x12 mm, 0.4 mm	–40 to +125° C
D211DCV	128 MB DDR3	QFN100, 12x12 mm, 0.4 mm	–20 to +105° C
D211DCX	128 MB DDR3	QFN100, 12x12 mm, 0.4 mm	–40 to +125° C
D213ECV	128 MB DDR3	QFN128, 12.3x12.3 mm, 0.35 mm	–20 to +105° C
D213ECX	128 MB DDR3	QFN128, 12.3x12.3 mm, 0.35 mm	–40 to +125° C

Table 3–2 Product Comparison

Item	D211BBV/ D211BBX D211BCV/ D211BCX	D211DBV/ D211DBX D211DCV/ D211DCX	D213ECV/ D213ECX
CPU	C906 600MHz@1.2V	C906 600MHz@1.2V	C906 600MHz@1.2V
Safety	Support	Support	Support
RGB	x 1	x 1	x 1
LVDS	x 2	x 2	x 2
MIPI DSI	x 1	x 1	x 1
RTP	x 1	x 1	x 1
DVP	x 1	x 1	x 1
RTC	x 1	x 1	x 1
eMMC 4.41	x 1	x 1	x 1
SD 2.0	x 1	x 1	x 1
SDIO 2.0	x 1	x 1	x 1
AMIC	x 1	x 1	x 1
DMIC	x 2	x 2	x 2
I2S	x 1	x 1	x 2
DSPK	x 2	x 2	x 2
SPI	x 2	x 2	x 2
QSPI	x 2	x 2	x 2
UART	x 8	x 8	x 8
I2C	x 4	x 4	x 4
CAN	x 2	x 2	x 2
CIR	x 1	x 1	x 1
EMAC–100M	x 1	x 2	x 2

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Table 3–2 Product Comparison (continued)

Item	D211BBV/ D211BBX D211BCV/ D211BCX	D211DBV/ D211DBX D211DCV/ D211DCX	D213ECV/ D213ECX
GMAC–1000M	–	–	x 2
USB2.0	x 1	x 2	x 2
PWM	x 4 (8 ch)	x 4 (8 ch)	x 4 (8 ch)
EPWM	x 6 (12 ch)	x 6 (12 ch)	x 6 (12 ch)
CAP	x 3	x 3	x 3
QEP	x 2	x 2	x 2
ADC	x 2 (7 ch)	x 2 (7 ch)	x 2 (12 ch)

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4. Electrical Features

4.1. Operating Conditions

4.1.1. Maximum Values

Symbol	Description	Minimum	Maximum	Unit
Tstg	Storage temperature	–40	125	℃
VCC33_IO0	GPIOA/ GPIOB/ GPIOE power source	–0.3	3.6	V
VCC33_IO1	GPIOC/ GPIOD/ GPIOF power source	–0.3	3.6	V
RTC_VCOIN	RTC power source	–0.3	3.6	V
VCC_DRAM	DRAW power source	–0.3	1.85	V
VDD11_SYS	Kernel and system power supply	–0.3	1.32	V
Iio	IO input/output current	–55	60	mA

4.1.2. Recommended Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit
Tj	Junction temperature	–40	–	125	℃
Ta	Ambient temperature	–40	–	105	℃
VCC33_IO0	GPIOA/ GPIOB/ GPIOE power source	3.0	3.3	3.6	V
VCC33_IO1	GPIOC/ GPIOD/ GPIOF power source	3.0	3.3	3.6	V
RTC_VCOIN	RTC power source	2.7	3.0	VCC33_IO1	V
VCC_DRAM	DRAW power source	1.35	1.5/ 1.8	1.85	V
VDD_SYS	Kernel and system power supply	0.9	1.1/ 1.2	1.32	V

4.2. RTC Power Supply

RTC is powered by VCC33_IO1 and VCOIN.In system design, the internal circuit automatically checks and compares the voltages of VCC33_IO1 and VCOIN, and chooses the circuit with the higher voltage for power supply.

- When power is on, the typical voltage is 3.3 V for VCC33_IO1 and 3.0V for VCOIN which is powered by button cells. In this case, the voltage of VCC33_IO is higher than that of VCOIN, and thus RTC is powered by VCC33_IO1.
- When power is off, VCC33_IO1 is not powered, and VCOIN becomes the only power source. The typical voltage powered by button cells is 3.0 V, and thus RTC is powered by VCOIN. In this case, the typical operating current of RTC is 3.3 uA, which helps to prolong the service life of button cells.

For external power supply, VCOIN needs to be connected with an RC delay power–on circuit (10 KΩ / 0.1 uF). This solution can ensure a smooth transition of power supply for RTC during power–on or power–off, and avoid damage to RTC caused by sudden voltage changes.

4.3. Power–on/Power–off Sequence and Reset

4.3.1. Power–on/Power–off Sequence

There is no power–on and power–off sequence requirement for VCC33_IO, VCC_DRAM and VDD11_SYS. The rising edge working at VCC33_IO shall be detected after 150 us.

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4.3.2. Reset Source

When any of the following reset conditions is met, the chip will reset:

- SYS power-on reset: a reset is triggered when VCC33_IO0 and VDD11_SYS are powered on. The system automatically releases the reset within 10 ms after power on.
- RTC power-on reset: a reset is automatically completed when RTC powers on (by VCC33_IO1 and VCOIN).
- External pin reset: a reset is triggered when the RESETN pin is driven low for over 2ms.
- Debugger reset: a reset is immediately triggered upon receiving the RESET signal from JTAG IO.
- Watchdog reset: when the reset is enabled, a reset is immediately triggered when the configured timeout reset conditions are met in WDOG.

4.4. Built-in LDO Electrical Features

4.4.1. LDO30

The built-in LDO30 (VCC30_ANA) is used for power supply of analog subsystems and GPADC/ PSADC/ Audio ADC. LDO30 can aslo be used as the referenced voltage for PSADC and Its electrical characteristics are as follows:

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{LDO30}	Output voltage	2.95	3.00	3.05	V
Io	Output current	–	–	100	mA
Co	External decoupling capacitor	–	1	–	uF

4.4.2. LDO25

The built-in LDO25 is used for power supply of DRAM controllers and eFuse. Its electrical characteristics are as follows:

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{LDO25}	Output voltage	2.45	–	2.55	V
Io	Output current	–	–	50	mA
Co	External decoupling capacitor	–	1	–	uF

4.4.3. LDO1x

The built-in LDO1x is configurable and its electrical characteristics are as follows:

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{LDO1x}	Output voltage	1.35	–	1.85	V
Io	Output current	–	–	500	mA
Co	External decoupling capacitor	–	1	–	uF

4.5. Clock

4.5.1. External Clock Source

- 32.768 KHz clock: for low frequency and RTC.
- 24.000 MHz clock: for low frequency and RTC.

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Symbol	Description	Minimum	Typical	Maximum	Unit
OSC_24M	PLL clock source	–	24	–	MHz
OSC_32K	RTC clock source	–	32768	–	Hz

4.6. IO Electrical Features

4.6.1. IO DC Electrical Features

Symbol	Description	Minimum	Typical	Maximum	Unit
VIH	High-level input voltage	0.7 * VCC33_IO	–	VCC33_IO + 0.3	V
VIL	Low-level input voltage	-0.3	–	0.3 * VCC33_IO	V
RPU	Pullup resistor	–	33	–	KΩ
RPD	Pulldown resistor	–	33	–	KΩ
IIH	High-level input current	–	–	10	uA
IIL	Low-level input current	–	–	10	uA
VOH	High-level output voltage	VCC33_IO + 0.3	–	For VCC33_IO	V
VOL	Low-level output voltage	0	–	0.3	V
IOH	High-level output current	8	–	60	mA
IOL	Low-level output current	8	–	55	mA
IOZ	Tri-stated output leakage current	-10	–	10	uA
CIN	Input capacitance	–	–	5	pF
COUT	Output capacitance	–	–	5	pF

4.6.2. IO AC Electrical Features

Symbol	Description	Test Conditions	Minimum	Typical	Maximum	Unit
fmax	Maximum frequency	6pF of load capacitance	–	–	150	MHz
TR230	Rise time	Time between VOL and VOH	–	–	1.6	ns
tf	Fall time	Time between VOH and VOL	–	–	1.6	ns

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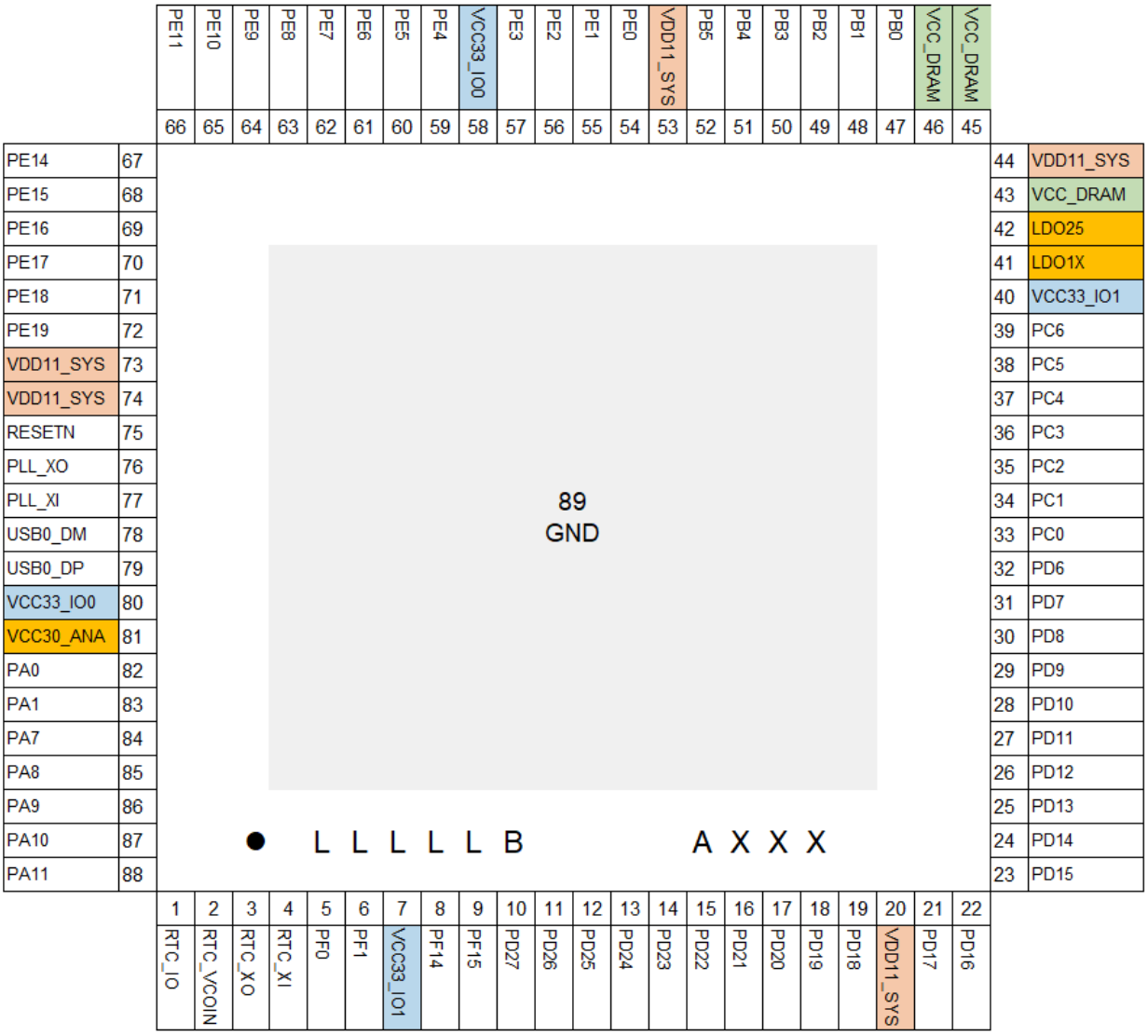
5. Package Information

5.1. Pin Distribution

5.1.1. D211BB/ D211BC QFN88



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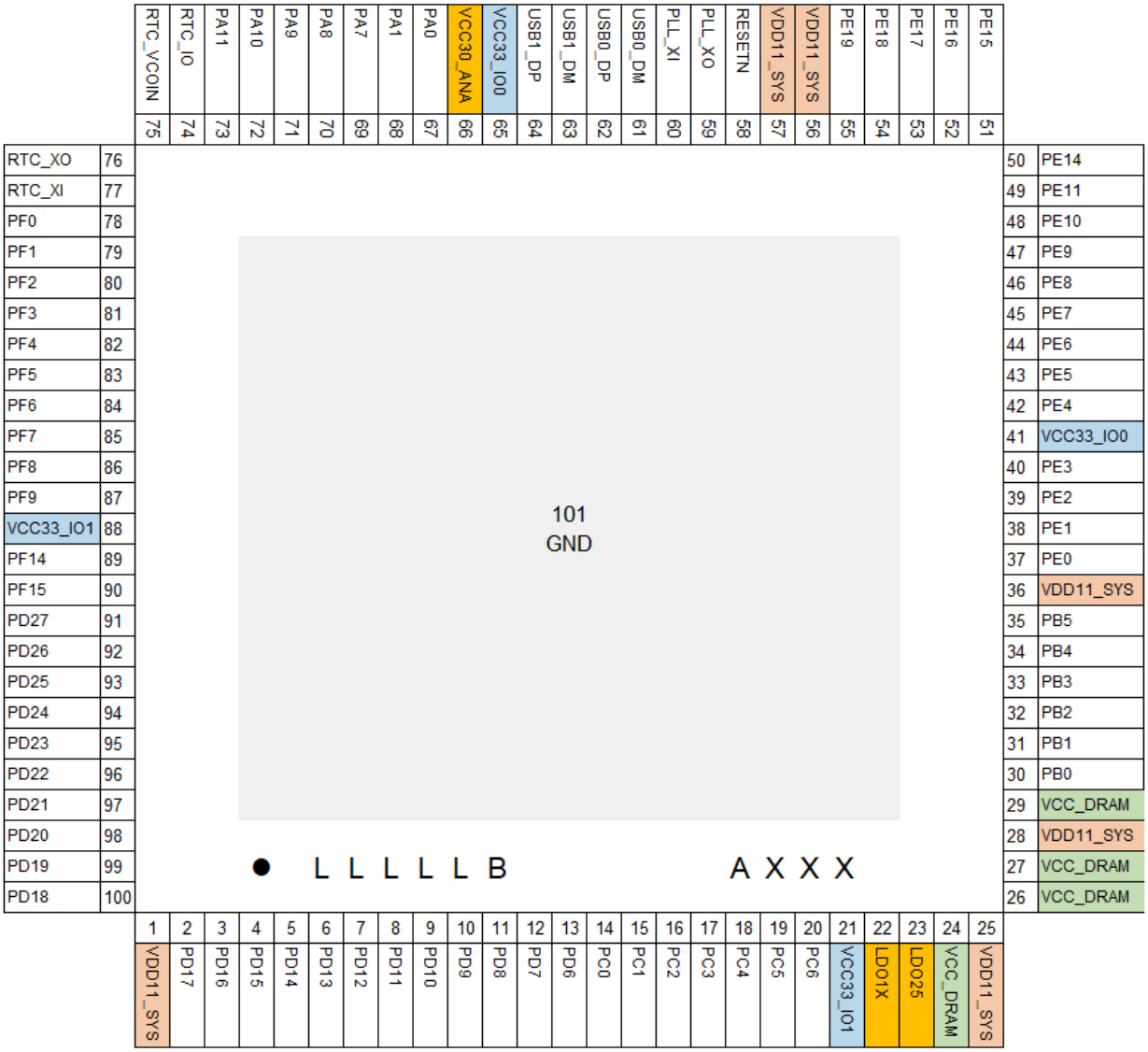
5.1.2. D211DB/ D211DC QFN100



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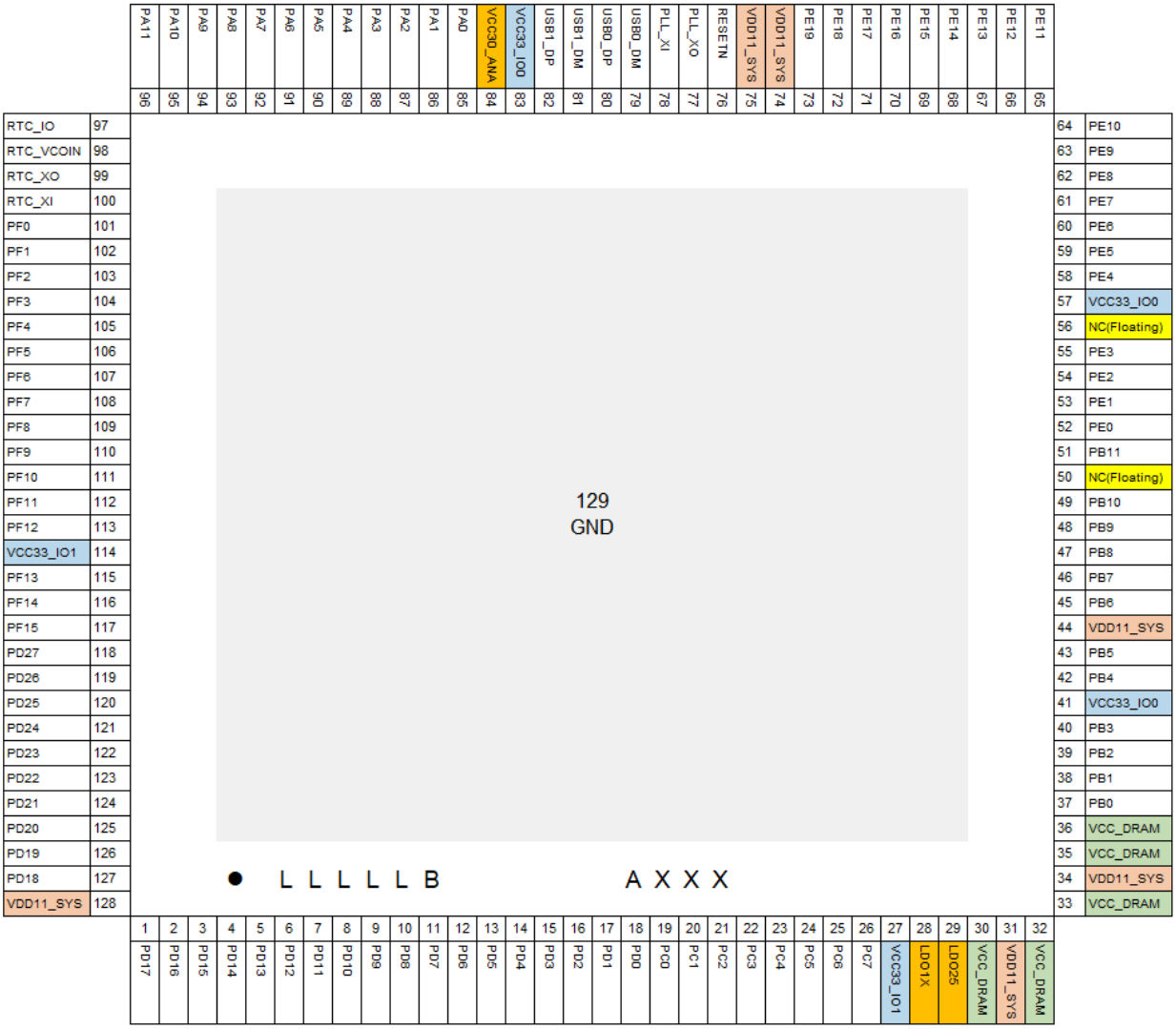
5.1.3. D213EC QFN128



LLLLLB: LLLLL indicates bacth number, and B is a fixed letter.

AXXX: XXX indictaes date code, and A is a fixed letter.

5.2. Pin Attributes

Note:

- [1]: Serial number of pin in the package
- [2]: Name of pin in the package
- [3]: Signal Type, to indicate signal directions
  - I – Input
  - O – Output
  - I/O – Input/ Output
  - A – Analog
  - AI – Analog Input
  - AO – Analog Output

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◦ P – Power

◦ G – Ground

• [4]: Pin reset status, PU means pullup, PD means pulldown, and Z means high impedance state.

• [5]: PU/PD means there are internal pullup and pulldown resistors which can be enable and disable by software.

• [6]: Default output current. For GPIO, the default output current is 20 mA and the maximum is 50 mA.

• [7]: Power source

5.2.1. D211BB/ D211BC QFN88

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
GPIO A						
82	PA0	I/O	Z	PU/PD	20	VCC33_IO0
83	PA1	I/O	Z	PU/PD	20	VCC33_IO0
84	PA7	I/O	Z	PU/PD	20	VCC33_IO0
85	PA8	I/O	PU	PU/PD	20	VCC33_IO0
86	PA9	I/O	PU	PU/PD	20	VCC33_IO0
87	PA10	I/O	PU	PU/PD	20	VCC33_IO0
88	PA11	I/O	PU	PU/PD	20	VCC33_IO0
GPIO B						
47	PB0	I/O	Z	PU/PD	20	VCC33_IO0
48	PB1	I/O	Z	PU/PD	20	VCC33_IO0
49	PB2	I/O	Z	PU/PD	20	VCC33_IO0
50	PB3	I/O	Z	PU/PD	20	VCC33_IO0
51	PB4	I/O	Z	PU/PD	20	VCC33_IO0
52	PB5	I/O	Z	PU/PD	20	VCC33_IO0
GPIO C						
33	PC0	I/O	Z	PU/PD	20	VCC33_IO1
34	PC1	I/O	Z	PU/PD	20	VCC33_IO1
35	PC2	I/O	Z	PU/PD	20	VCC33_IO1
36	PC3	I/O	Z	PU/PD	20	VCC33_IO1
37	PC4	I/O	Z	PU/PD	20	VCC33_IO1
38	PC5	I/O	Z	PU/PD	20	VCC33_IO1
39	PC6	I/O	Z	PU/PD	20	VCC33_IO1
GPIO D						
32	PD6	I/O	Z	PU/PD	20	VCC33_IO1
31	PD7	I/O	Z	PU/PD	20	VCC33_IO1
30	PD8	I/O	Z	PU/PD	20	VCC33_IO1
29	PD9	I/O	Z	PU/PD	20	VCC33_IO1
28	PD10	I/O	Z	PU/PD	20	VCC33_IO1
27	PD11	I/O	Z	PU/PD	20	VCC33_IO1

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
26	PD12	I/O	Z	PU/PD	20	VCC33_IO1
25	PD13	I/O	Z	PU/PD	20	VCC33_IO1
24	PD14	I/O	Z	PU/PD	20	VCC33_IO1
23	PD15	I/O	Z	PU/PD	20	VCC33_IO1
22	PD16	I/O	Z	PU/PD	20	VCC33_IO1
21	PD17	I/O	Z	PU/PD	20	VCC33_IO1
19	PD18	I/O	Z	PU/PD	20	VCC33_IO1
18	PD19	I/O	Z	PU/PD	20	VCC33_IO1
17	PD20	I/O	Z	PU/PD	20	VCC33_IO1
16	PD21	I/O	Z	PU/PD	20	VCC33_IO1
15	PD22	I/O	Z	PU/PD	20	VCC33_IO1
14	PD23	I/O	Z	PU/PD	20	VCC33_IO1
13	PD24	I/O	Z	PU/PD	20	VCC33_IO1
12	PD25	I/O	Z	PU/PD	20	VCC33_IO1
11	PD26	I/O	Z	PU/PD	20	VCC33_IO1
10	PD27	I/O	Z	PU/PD	20	VCC33_IO1
GPIO E						
54	PE0	I/O	Z	PU/PD	20	VCC33_IO0
55	PE1	I/O	Z	PU/PD	20	VCC33_IO0
56	PE2	I/O	Z	PU/PD	20	VCC33_IO0
57	PE3	I/O	Z	PU/PD	20	VCC33_IO0
59	PE4	I/O	Z	PU/PD	20	VCC33_IO0
60	PE5	I/O	Z	PU/PD	20	VCC33_IO0
61	PE6	I/O	Z	PU/PD	20	VCC33_IO0
62	PE7	I/O	Z	PU/PD	20	VCC33_IO0
63	PE8	I/O	Z	PU/PD	20	VCC33_IO0
64	PE9	I/O	Z	PU/PD	20	VCC33_IO0
65	PE10	I/O	Z	PU/PD	20	VCC33_IO0
66	PE11	I/O	Z	PU/PD	20	VCC33_IO0
67	PE14	I/O	Z	PU/PD	20	VCC33_IO0
68	PE15	I/O	Z	PU/PD	20	VCC33_IO0
69	PE16	I/O	Z	PU/PD	20	VCC33_IO0
70	PE17	I/O	Z	PU/PD	20	VCC33_IO0
71	PE18	I/O	Z	PU/PD	20	VCC33_IO0
72	PE19	I/O	Z	PU/PD	20	VCC33_IO0
GPIO F						
5	PF0	I/O	Z	PU/PD	20	VCC33_IO1
6	PF1	I/O	Z	PU/PD	20	VCC33_IO1
8	PF14	I/O	Z	PU/PD	20	VCC33_IO1
9	PF15	I/O	Z	PU/PD	20	VCC33_IO1
RTC						

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
1	RTC_IO	OD	–	–	–	–
2	RTC_VCOIN	P	–	–	–	–
3	RTC_XO	O	–	–	–	–
4	RTC_XI	I	–	–	–	–
PLL						
75	RESET	I	–	–	–	–
76	PLL_XO	O	–	–	–	–
77	PLL_XI	I	–	–	–	–
USB						
78	USB0_DM	A	–	–	–	–
79	USB0_DP	A	–	–	–	–
Power						
58,80	VCC33_IO0	P	–	–	–	–
7,40	VCC33_IO1	P	–	–	–	–
81	VCC30_ANA	P	–	–	–	–
42	LDO25	P	–	–	–	–
41	LDO1X	P	–	–	–	–
43, 45, 46	VCC_DRAM	P	–	–	–	–
20, 44, 53, 73, 74	VDD11_SYS	P	–	–	–	–
89	GND	P	–	–	–	–

5.2.2. D211DB/ D211DC QFN100

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
GPIOA						
67	PA0	I/O	Z	PU/PD	20	VCC33_IO0
68	PA1	I/O	Z	PU/PD	20	VCC33_IO0
69	PA7	I/O	Z	PU/PD	20	VCC33_IO0
70	PA8	I/O	PU	PU/PD	20	VCC33_IO0
71	PA9	I/O	PU	PU/PD	20	VCC33_IO0
72	PA10	I/O	PU	PU/PD	21	VCC33_IO0
73	PA11	I/O	PU	PU/PD	20	VCC33_IO0
GPIO B						
30	PB0	I/O	Z	PU/PD	20	VCC33_IO0
31	PB1	I/O	Z	PU/PD	20	VCC33_IO0
32	PB2	I/O	Z	PU/PD	20	VCC33_IO0
33	PB3	I/O	Z	PU/PD	20	VCC33_IO0
34	PB4	I/O	Z	PU/PD	20	VCC33_IO0
35	PB5	I/O	Z	PU/PD	20	VCC33_IO0
GPIO C						
14	PC0	I/O	Z	PU/PD	20	VCC33_IO1

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
15	PC1	I/O	Z	PU/PD	20	VCC33_IO1
16	PC2	I/O	Z	PU/PD	20	VCC33_IO1
17	PC3	I/O	Z	PU/PD	20	VCC33_IO1
18	PC4	I/O	Z	PU/PD	20	VCC33_IO1
19	PC5	I/O	Z	PU/PD	20	VCC33_IO1
20	PC6	I/O	Z	PU/PD	20	VCC33_IO1
GPIO D						
13	PD6	I/O	Z	PU/PD	20	VCC33_IO1
12	PD7	I/O	Z	PU/PD	20	VCC33_IO1
11	PD8	I/O	Z	PU/PD	20	VCC33_IO1
10	PD9	I/O	Z	PU/PD	20	VCC33_IO1
9	PD10	I/O	Z	PU/PD	20	VCC33_IO1
8	PD11	I/O	Z	PU/PD	20	VCC33_IO1
7	PD12	I/O	Z	PU/PD	20	VCC33_IO1
6	PD13	I/O	Z	PU/PD	20	VCC33_IO1
5	PD14	I/O	Z	PU/PD	20	VCC33_IO1
4	PD15	I/O	Z	PU/PD	20	VCC33_IO1
3	PD16	I/O	Z	PU/PD	20	VCC33_IO1
2	PD17	I/O	Z	PU/PD	20	VCC33_IO1
100	PD18	I/O	Z	PU/PD	20	VCC33_IO1
99	PD19	I/O	Z	PU/PD	20	VCC33_IO1
98	PD20	I/O	Z	PU/PD	20	VCC33_IO1
97	PD21	I/O	Z	PU/PD	20	VCC33_IO1
96	PD22	I/O	Z	PU/PD	20	VCC33_IO1
95	PD23	I/O	Z	PU/PD	20	VCC33_IO1
94	PD24	I/O	Z	PU/PD	20	VCC33_IO1
93	PD25	I/O	Z	PU/PD	20	VCC33_IO1
92	PD26	I/O	Z	PU/PD	20	VCC33_IO1
91	PD27	I/O	Z	PU/PD	20	VCC33_IO1
GPIO E						
37	PE0	I/O	Z	PU/PD	20	VCC33_IO0
38	PE1	I/O	Z	PU/PD	20	VCC33_IO0
39	PE2	I/O	Z	PU/PD	20	VCC33_IO0
40	PE3	I/O	Z	PU/PD	20	VCC33_IO0
42	PE4	I/O	Z	PU/PD	20	VCC33_IO0
43	PE5	I/O	Z	PU/PD	20	VCC33_IO0
44	PE6	I/O	Z	PU/PD	20	VCC33_IO0
45	PE7	I/O	Z	PU/PD	20	VCC33_IO0
46	PE8	I/O	Z	PU/PD	20	VCC33_IO0
47	PE9	I/O	Z	PU/PD	20	VCC33_IO0
48	PE10	I/O	Z	PU/PD	20	VCC33_IO0

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
49	PE11	I/O	Z	PU/PD	20	VCC33_IO0
50	PE14	I/O	Z	PU/PD	20	VCC33_IO0
51	PE15	I/O	Z	PU/PD	20	VCC33_IO0
52	PE16	I/O	Z	PU/PD	20	VCC33_IO0
53	PE17	I/O	Z	PU/PD	20	VCC33_IO0
54	PE18	I/O	Z	PU/PD	20	VCC33_IO0
55	PE19	I/O	Z	PU/PD	20	VCC33_IO0
GPIO F						
78	PF0	I/O	Z	PU/PD	20	VCC33_IO1
79	PF1	I/O	Z	PU/PD	20	VCC33_IO1
80	PF2	I/O	Z	PU/PD	20	VCC33_IO1
81	PF3	I/O	Z	PU/PD	20	VCC33_IO1
82	PF4	I/O	Z	PU/PD	20	VCC33_IO1
83	PF5	I/O	Z	PU/PD	20	VCC33_IO1
84	PF6	I/O	Z	PU/PD	20	VCC33_IO1
85	PF7	I/O	Z	PU/PD	20	VCC33_IO1
86	PF8	I/O	Z	PU/PD	20	VCC33_IO1
87	PF9	I/O	Z	PU/PD	20	VCC33_IO1
89	PF14	I/O	Z	PU/PD	20	VCC33_IO1
90	PF15	I/O	Z	PU/PD	20	VCC33_IO1
RTC						
74	RTC_IO	OD	–	–	–	–
75	RTC_VCOIN	P	–	–	–	–
76	RTC_XO	O	–	–	–	–
77	RTC_XI	I	–	–	–	–
PLL						
58	RESET	I	–	–	–	–
59	PLL_XO	O	–	–	–	–
60	PLL_XI	I	–	–	–	–
USB						
61	USB0_DM	A	–	–	–	–
62	USB0_DP	A	–	–	–	–
63	USB1_DM	A	–	–	–	–
64	USB1_DP	A	–	–	–	–
Power						
41,65	VCC33_IO0	P	–	–	–	–
21,88	VCC33_IO1	P	–	–	–	–
66	VCC30_ANA	P	–	–	–	–
23	LDO25	P	–	–	–	–
22	LDO1X	P	–	–	–	–
24, 26, 27, 29	VCC_DRAM	P	–	–	–	–

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
1,25, 28, 36, 56, 57	VDD11_SYS	P	–	–	–	–
101	GND	P	–	–	–	–

5.2.3. D213EC QFN128

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
GPIOA						
85	PA0	I/O	Z	PU/PD	20	VCC33_IO0
86	PA1	I/O	Z	PU/PD	20	VCC33_IO0
87	PA2	I/O	Z	PU/PD	20	VCC33_IO0
88	PA3	I/O	Z	PU/PD	20	VCC33_IO0
89	PA4	I/O	Z	PU/PD	20	VCC33_IO0
90	PA5	I/O	Z	PU/PD	20	VCC33_IO0
91	PA6	I/O	Z	PU/PD	20	VCC33_IO0
92	PA7	I/O	Z	PU/PD	20	VCC33_IO0
93	PA8	I/O	PU	PU/PD	20	VCC33_IO0
94	PA9	I/O	PU	PU/PD	20	VCC33_IO0
95	PA10	I/O	PU	PU/PD	20	VCC33_IO0
96	PA11	I/O	PU	PU/PD	20	VCC33_IO0
GPIO B						
37	PB0	I/O	Z	PU/PD	20	VCC33_IO0
38	PB1	I/O	Z	PU/PD	20	VCC33_IO0
39	PB2	I/O	Z	PU/PD	20	VCC33_IO0
40	PB3	I/O	Z	PU/PD	20	VCC33_IO0
42	PB4	I/O	Z	PU/PD	20	VCC33_IO0
43	PB5	I/O	Z	PU/PD	20	VCC33_IO0
45	PB6	I/O	Z	PU/PD	20	VCC33_IO0
46	PB7	I/O	Z	PU/PD	20	VCC33_IO0
47	PB8	I/O	Z	PU/PD	20	VCC33_IO0
48	PB9	I/O	Z	PU/PD	20	VCC33_IO0
49	PB10	I/O	Z	PU/PD	20	VCC33_IO0
51	PB11	I/O	Z	PU/PD	20	VCC33_IO0
50	NC	I/O	Z	PU/PD	20	VCC33_IO0
56	NC	I/O	Z	PU/PD	20	VCC33_IO0
GPIO C						
19	PC0	I/O	Z	PU/PD	20	VCC33_IO1
20	PC1	I/O	Z	PU/PD	20	VCC33_IO1
21	PC2	I/O	Z	PU/PD	20	VCC33_IO1
22	PC3	I/O	Z	PU/PD	20	VCC33_IO1
23	PC4	I/O	Z	PU/PD	20	VCC33_IO1
24	PC5	I/O	Z	PU/PD	20	VCC33_IO1

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
25	PC6	I/O	Z	PU/PD	20	VCC33_IO1
26	PC7	I/O	Z	PU/PD	20	VCC33_IO1
GPIO D						
18	PD0	I/O	Z	PU/PD	20	VCC33_IO1
17	PD1	I/O	Z	PU/PD	20	VCC33_IO1
16	PD2	I/O	Z	PU/PD	20	VCC33_IO1
15	PD3	I/O	Z	PU/PD	20	VCC33_IO1
14	PD4	I/O	Z	PU/PD	20	VCC33_IO1
13	PD5	I/O	Z	PU/PD	20	VCC33_IO1
12	PD6	I/O	Z	PU/PD	20	VCC33_IO1
11	PD7	I/O	Z	PU/PD	20	VCC33_IO1
10	PD8	I/O	Z	PU/PD	20	VCC33_IO1
9	PD9	I/O	Z	PU/PD	20	VCC33_IO1
8	PD10	I/O	Z	PU/PD	20	VCC33_IO1
7	PD11	I/O	Z	PU/PD	20	VCC33_IO1
6	PD12	I/O	Z	PU/PD	20	VCC33_IO1
5	PD13	I/O	Z	PU/PD	20	VCC33_IO1
4	PD14	I/O	Z	PU/PD	20	VCC33_IO1
3	PD15	I/O	Z	PU/PD	20	VCC33_IO1
2	PD16	I/O	Z	PU/PD	20	VCC33_IO1
1	PD17	I/O	Z	PU/PD	20	VCC33_IO1
127	PD18	I/O	Z	PU/PD	20	VCC33_IO1
126	PD19	I/O	Z	PU/PD	20	VCC33_IO1
125	PD20	I/O	Z	PU/PD	20	VCC33_IO1
124	PD21	I/O	Z	PU/PD	20	VCC33_IO1
123	PD22	I/O	Z	PU/PD	20	VCC33_IO1
122	PD23	I/O	Z	PU/PD	20	VCC33_IO1
121	PD24	I/O	Z	PU/PD	20	VCC33_IO1
120	PD25	I/O	Z	PU/PD	20	VCC33_IO1
119	PD26	I/O	Z	PU/PD	20	VCC33_IO1
118	PD27	I/O	Z	PU/PD	20	VCC33_IO1
GPIO E						
52	PE0	I/O	Z	PU/PD	20	VCC33_IO0
53	PE1	I/O	Z	PU/PD	20	VCC33_IO0
54	PE2	I/O	Z	PU/PD	20	VCC33_IO0
55	PE3	I/O	Z	PU/PD	20	VCC33_IO0
58	PE4	I/O	Z	PU/PD	20	VCC33_IO0
59	PE5	I/O	Z	PU/PD	20	VCC33_IO0
60	PE6	I/O	Z	PU/PD	20	VCC33_IO0
61	PE7	I/O	Z	PU/PD	20	VCC33_IO0
62	PE8	I/O	Z	PU/PD	20	VCC33_IO0

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
63	PE9	I/O	Z	PU/PD	20	VCC33_IO0
64	PE10	I/O	Z	PU/PD	20	VCC33_IO0
65	PE11	I/O	Z	PU/PD	20	VCC33_IO0
66	PE12	I/O	Z	PU/PD	20	VCC33_IO0
67	PE13	I/O	Z	PU/PD	20	VCC33_IO0
68	PE14	I/O	Z	PU/PD	20	VCC33_IO0
69	PE15	I/O	Z	PU/PD	20	VCC33_IO0
70	PE16	I/O	Z	PU/PD	20	VCC33_IO0
71	PE17	I/O	Z	PU/PD	20	VCC33_IO0
72	PE18	I/O	Z	PU/PD	20	VCC33_IO0
73	PE19	I/O	Z	PU/PD	20	VCC33_IO0
GPIO F						
101	PF0	I/O	Z	PU/PD	20	VCC33_IO1
102	PF1	I/O	Z	PU/PD	20	VCC33_IO1
103	PF2	I/O	Z	PU/PD	20	VCC33_IO1
104	PF3	I/O	Z	PU/PD	20	VCC33_IO1
105	PF4	I/O	Z	PU/PD	20	VCC33_IO1
106	PF5	I/O	Z	PU/PD	20	VCC33_IO1
107	PF6	I/O	Z	PU/PD	20	VCC33_IO1
108	PF7	I/O	Z	PU/PD	20	VCC33_IO1
109	PF8	I/O	Z	PU/PD	20	VCC33_IO1
110	PF9	I/O	Z	PU/PD	20	VCC33_IO1
111	PF10	I/O	Z	PU/PD	20	VCC33_IO1
112	PF11	I/O	Z	PU/PD	20	VCC33_IO1
113	PF12	I/O	Z	PU/PD	20	VCC33_IO1
115	PF13	I/O	Z	PU/PD	20	VCC33_IO1
116	PF14	I/O	Z	PU/PD	20	VCC33_IO1
117	PF15	I/O	Z	PU/PD	20	VCC33_IO1
RTC						
97	RTC_IO	OD	–	–	–	–
98	RTC_VCOIN	P	–	–	–	–
99	RTC_XO	O	–	–	–	–
100	RTC_XI	I	–	–	–	–
PLL						
76	RESET	I	–	–	–	–
77	PLL_XO	O	–	–	–	–
78	PLL_XI	I	–	–	–	–
USB						
79	USB0_DM	A	–	–	–	–
80	USB0_DP	A	–	–	–	–
81	USB1_DM	A	–	–	–	–

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Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
82	USB1_DP	A	–	–	–	–
Power						
41, 57, 83	VCC33_IO0	P	–	–	–	–
27, 114	VCC33_IO1	P	–	–	–	–
84	VCC30_ANA	P	–	–	–	–
29	LDO25	P	–	–	–	–
28	LDO1X	P	–	–	–	–
30, 32, 33, 35, 36	VCC_DRAM	P	–	–	–	–
31, 34, 44, 74, 75, 128	VDD11_SYS	P	–	–	–	–
129	GND	P	–	–	–	–

5.3. Pin–Mux

Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
PA0	GPADC0	PSADC0	I2C0_SCL	UART0_TX	AMIC_IN	IR_TX	–
PA1	GPADC1	PSADC1	I2C0_SDA	UART0_RX	AMIC_BIAS	IR_RX	–
PA2	GPADC2	PSADC2	–	UART0_RTS	–	–	–
PA3	GPADC3	PSADC3	–	UART0_CTS	–	–	–
PA4	GPADC4	PSADC4	–	UART1_TX	–	–	–
PA5	GPADC5	PSADC5	–	UART1_RX	–	–	–
PA6	GPADC6	PSADC6	I2C1_SCL	UART1_RTS	–	–	–
PA7	GPADC7	PSADC7	I2C1_SDA	UART1_CTS	–	–	–
PA8	RTP_XP	PSADC8	I2C2_SCL	UART2_TX	JTAG_DO	–	–
PA9	RTP_YP	PSADC9	I2C2_SDA	UART2_RX	JTAG_DI	–	–
PA10	RTP_XN	PSADC10	I2C3_SCL	UART2_RTS	JTAG_MS	–	–
PA11	RTP_YN	PSADC11	I2C3_SDA	UART2_CTS	JTAG_CK	–	–
PB0	SDC0_CMD	SPI0_HOLD	I2C1_SCL	UART7_TX	–	–	–
PB1	SDC0_CLK	SPI0_WP	I2C1_SDA	UART7_RX	–	–	–
PB2	SDC0_D3	SPI0_CS	–	–	–	–	–
PB3	SDC0_D0	SPI0_MISO	–	–	–	–	–
PB4	SDC0_D1	SPI0_MOSI	–	–	–	–	–
PB5	SDC0_D2	SPI0_CLK	–	–	–	–	–
PB6	SDC0_D4	SPI1_HOLD	I2C2_SCL	UART4_TX	–	CLK_OUT2	CLK_OUT3
PB7	SDC0_D5	SPI1_WP	I2C2_SDA	UART4_RX	–	–	–
PB8	SDC0_D6	SPI1_CS0	UART4_RTS	UART5_TX	–	IR_RX	–
PB9	SDC0_D7	SPI1_MISO	UART6_RTS	UART5_RX	–	IR_TX	–
PB10	SDC0_DS	SPI1_MOSI	–	UART6_TX	–	–	–
PB11	SDC0_RST	SPI1_CLK	–	UART6_RX	–	–	–
PC0	SDC1_D1	LCD_D5	SPI2_CLK	UART1_TX	JTAG_MS	PWM0_A	–
PC1	SDC1_D0	LCD_D4	SPI2_CS	UART1_RX	JTAG_DI	PWM0_B	–
PC2	SDC1_CLK	LCD_D3	SPI2_MOSI	UART1_RTS	UART0_TX	PWM1_A	–
PC3	SDC1_CMD	LCD_D2	SPI2_MISO	UART2_TX	JTAG_DO	PWM1_B	–

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Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
PC4	SDC1_D3	LCD_D1	–	UART2_RX	UART0_RX	PWM2_A	–
PC5	SDC1_D2	LCD_D0	UART2_RTS	UART3_TX	JTAG_CK	PWM2_B	–
PC6	SDC1_DET	CLK_OUT0	DE_TE	UART3_RX	–	PWM3_A	–
PC7	–	–	–	UART3_RTS	–	PWM3_B	–
PD0	LCD_D0	SPI2_CLK	–	–	PBUS_AD0	PWM0_A	–
PD1	LCD_D1	SPI2_CS	–	–	PBUS_AD1	PWM0_B	–
PD2	LCD_D2	SPI2_MOSI	DE_TE	–	PBUS_AD2	PWM1_A	–
PD3	LCD_D3	SPI3_CLK	–	–	PBUS_AD3	PWM1_B	–
PD4	LCD_D4	SPI3_CS0	–	–	PBUS_AD4	PWM2_A	–
PD5	LCD_D5	SPI3_MOSI	–	–	PBUS_AD5	PWM2_B	–
PD6	LCD_D6	SPI3_MISO	I2C0_SCL	UART1_TX	PBUS_AD6	–	–
PD7	LCD_D7	SPI2_MISO	I2C0_SDA	UART1_RX	PBUS_AD7	–	–
PD8	LCD_D8	LVDS1_D0N	SPI1_HOLD	UART2_TX	PBUS_AD8	EPWM0_A	–
PD9	LCD_D9	LVDS1_D0P	SPI1_WP	UART2_RX	PBUS_AD9	EPWM0_B	–
PD10	LCD_D10	LVDS1_D1N	SPI1_CS0	UART3_TX	PBUS_AD10	EPWM1_A	–
PD11	LCD_D11	LVDS1_D1P	SPI1_MISO	UART3_RX	PBUS_AD11	EPWM1_B	–
PD12	LCD_D12	LVDS1_D2N	SPI1_MOSI	UART4_TX	PBUS_AD12	EPWM2_A	–
PD13	LCD_D13	LVDS1_D2P	SPI1_CLK	UART4_RX	PBUS_AD13	EPWM2_B	–
PD14	LCD_D14	LVDS1_CKN	SPI3_CLK	CAP0	PBUS_AD14	QEP0_H0	–
PD15	LCD_D15	LVDS1_CKP	SPI3_CS0	CAP1	PBUS_AD15	QEP0_H1	–
PD16	LCD_D16	LVDS1_D3N	SPI3_MOSI	CAP2	PBUS_CLK	QEP0_H2	–
PD17	LCD_D17	LVDS1_D3P	SPI3_MISO	–	PBUS_NCS	QEP0_A	–
PD18	LCD_D18	LVDS0_D0N	DSI_D0N	I2C1_SCL	PBUS_NADV	QEP0_B	–
PD19	LCD_D19	LVDS0_D0P	DSI_D0P	I2C1_SDA	PBUS_NWE	QEP0_I	–
PD20	LCD_D20	LVDS0_D1N	DSI_D1N	UART7_TX	PBUS_NOE	QEP0_S	–
PD21	LCD_D21	LVDS0_D1P	DSI_D1P	UART7_RX	CLK_OUT0	–	–
PD22	LCD_D22	LVDS0_D2N	DSI_CKN	I2C3_SCL	UART6_TX	–	–
PD23	LCD_D23	LVDS0_D2P	DSI_CKP	I2C3_SDA	UART6_RX	–	–
PD24	LCD_DCLK	LVDS0_CKN	DSI_D2N	UART5_TX	SPI1_CLK	–	–
PD25	LCD_HS	LVDS0_CKP	DSI_D2P	UART5_RX	SPI1_CS0	–	–
PD26	LCD_VS	LVDS0_D3N	DSI_D3N	PWM3_A	SPI1_MOSI	–	–
PD27	LCD_DE	LVDS0_D3P	DSI_D3P	PWM3_B	SPI1_MISO	–	RTC_32K
PE0	–	DVP_D0	I2C0_SCL	–	GMAC0_RXD1	EPWM3_A	PWM0_A
PE1	–	DVP_D1	I2C0_SDA	–	GMAC0_RXD0	EPWM3_B	PWM0_B
PE2	–	DVP_D2	CAN0_TX	UART4_TX	GMAC0_RXCTL	EPWM4_A	PWM1_A
PE3	–	DVP_D3	CAN0_RX	UART4_RX	GMAC0_CLKIN	EPWM4_B	PWM1_B
PE4	–	DVP_D4	CAN1_TX	UART5_TX	GMAC0_TXD1	EPWM5_A	PWM2_A
PE5	–	DVP_D5	CAN1_RX	UART5_RX	GMAC0_TXD0	EPWM5_B	PWM2_B
PE6	DSPK0	DVP_D6	UART5_RTS	UART6_TX	GMAC0_TXCK	QEP1_H0	CAP0
PE7	DSPK1	DVP_D7	UART7_RTS	UART6_RX	GMAC0_TXCTL	QEP1_H1	CAP1
PE8	I2S0_MCLK	DVP_CK	UART6_RTS	UART7_TX	GMAC0_MDC	QEP1_H2	CAP2
PE9	I2S0_BCLK	DVP_HS	UART6_CTS	UART7_RX	GMAC0_MDIO	QEP1_A	–

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Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
PE10	I2S0_LRCK	DVP_VS	DSPK0	–	CLK_OUT2	QEP1_B	–
PE11	I2S0_DOUT	I2S0_DIN	DSPK1	CLK_OUT1	GMAC0_RXD3	QEP1_I	–
PE12	I2S0_DIN	SPI3_CLK	DMIC_CLK	I2C2_SCL	GMAC0_RXD2	QEP1_S	–
PE13	–	SPI3_CS0	DMIC_D0	I2C2_SDA	GMAC0_RXCK	CAP0	–
PE14	–	SPI3_MOSI	–	UART3_TX	GMAC0_TXD3	CAP1	–
PE15	–	SPI3_MISO	–	UART3_RX	GMAC0_TXD2	CAP2	–
PE16	–	SPI0_CLK	CAN0_TX	I2C3_SCL	GMAC0_TRIG	–	–
PE17	–	SPI0_CS	CAN0_RX	I2C3_SDA	GMAC0_PPSO	–	–
PE18	–	SPI0_MOSI	CAN1_TX	PWM3_A	GMAC1_TRIG	–	–
PE19	–	SPI0_MISO	CAN1_RX	PWM3_B	GMAC1_PPSO	–	–
PF0	SDC2_D1	SPI2_CLK	–	UART5_TX	GMAC1_RXD1	PBUS_AD0	–
PF1	SDC2_D0	SPI2_CS	–	UART5_RX	GMAC1_RXD0	PBUS_AD1	–
PF2	SDC2_CLK	SPI2_MOSI	–	UART5_RTS	GMAC1_RXCTL	PBUS_AD2	–
PF3	SDC2_CMD	SPI2_MISO	–	UART5_CTS	GMAC1_CLKIN	PBUS_AD3	–
PF4	SDC2_D3	–	–	UART6_TX	GMAC1_TXD1	PBUS_AD4	–
PF5	SDC2_D2	–	–	UART6_RX	GMAC1_TXD0	PBUS_AD5	–
PF6	–	–	–	UART7_TX	GMAC1_TXCK	PBUS_AD6	–
PF7	–	–	–	UART7_RX	GMAC1_TXCTL	PBUS_AD7	–
PF8	–	–	–	UART7_RTS	GMAC1_MDC	PBUS_AD8	–
PF9	–	–	–	UART7_CTS	GMAC1_MDIO	PBUS_AD9	–
PF10	I2S1_MCLK	I2S1_DIN	–	UART3_CTS	CLK_OUT3	PBUS_AD10	–
PF11	I2S1_BCLK	–	PBUS_AD11	UART3_TX	GMAC1_RXD3	PBUS_CLK	–
PF12	I2S1_LRCK	–	UART4_RTS	UART3_RX	GMAC1_RXD2	PBUS_NCS	–
PF13	I2S1_DOUT	I2S1_DIN	UART4_CTS	UART3_RTS	GMAC1_RXCK	PBUS_NADV	–
PF14	I2S1_DIN	DSPK0	DMIC_D0	UART4_TX	GMAC1_TXD3	PBUS_NWE	–
PF15	DE_TE	DSPK1	DMIC_CLK	UART4_RX	GMAC1_TXD2	PBUS_NOE	–
PU0	USB0_DM	–	UART0_RX	UART1_RX	–	–	–
PU1	USB0_DP	–	UART0_TX	UART1_TX	–	–	–
PU2	USB1_DM	–	UART0_RX	UART2_RX	–	–	–
PU3	USB1_DP	–	UART0_TX	UART2_TX	–	–	–

5.3.1. Package Pin Description

5.3.1.1. D211BB/ D211BC QFN88 Package Pin Description

Table 5–1 D211BB (Sip DDR2)/ D211BC (Sip DDR3) QFN88 Package Pin Description

Pins	Definition	Signal Type	Function	Remark
RTC				
1	RTC_IO	OD	RTC 32K clock output	OD output, with an external pullup resistor. The pullup voltage must be lower than 5 V.
2	RTC_VCOIN	POWER	–	Can be floating if power–off protection is not considered. The internal diode can be powered by a 3.3–V source. If connected externally for power supply, a RC must be connected for power–on delay (10 KΩ/ 0.1 uF).

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Table 5–1 D211BB (Sip DDR2)/ D211BC (Sip DDR3) QFN88 Package Pin Description (continued)

Pins	Definition	Signal Type	Function	Remark
3	RTC_XO	OUTPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
4	RTC_XI	INPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
SYSTEM				
75	RESETN	INPUT	System Reset	Built in with a 30 KΩ pullup resistor and dithering filter which can be floating if not used. If an external capacitor is connected, the recommended load capacitance is less than 4.7 uF.
76	PLL_XO	OUTPUT	–	Connect with a 24–MHz crystal oscillator.
77	PLL_XI	INPUT	–	Connect with a 24–MHz crystal oscillator.
POWER				
58, 80	VCC33_IO0	POWER	IO Voltage	3.3 –V power supply
7, 40	VCC33_IO1	POWER	IO Voltage	3.3 –V power supply
81	VCC30_ANA	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
42	LDO25	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
41	LDO1x	POWER	Built–in LDO output	Configurable. Connect with a 1–uF bypass capacitor if needed. In this case, chip cooling must be considered.
43, 45, 46	VCC_DRAM	POWER	DRAW power source	DDR2 1.8 V power supplyDDR3 1.5 V power supply
20, 44, 53, 73, 74	VDD11_SYS	POWER	Chip Core Voltage	1.2 V power supply @600 MHz, 1.1 V power supply @504 MHz.
89	GND	POWER	–	GND Copper full–cover connection via stitching for cooling.

Table 5–2 D211BB (Sip DDR2) / D211BC (Sip DDR3) QFN88 Package Pin–mux

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
GPIO A								
82	PA0	GPADC0	PSADC0	I2C0_SCL	UART0_TX	AMIC_IN	IR_TX	–
83	PA1	GPADC1	PSADC1	I2C0_SDA	UART0_RX	AMIC_BIAS	IR_RX	–
84	PA7	GPADC7	PSADC7	I2C1_SDA	UART1_CTS	–	–	–
85	PA8	RTP_XP	PSADC8	I2C2_SCL	UART2_TX	JTAG_DO	–	–
86	PA9	RTP_YP	PSADC9	I2C2_SDA	UART2_RX	JTAG_DI	–	–
87	PA10	RTP_XN	PSADC10	I2C3_SCL	UART2_RTS	JTAG_MS	–	–
88	PA11	RTP_YN	PSADC11	I2C3_SDA	UART2_CTS	JTAG_CK	–	–
GPIO B								
47	PB0	SDC0_CMD	SPI0_HOLD	I2C1_SCL	UART7_TX	–	–	–
48	PB1	SDC0_CLK	SPI0_WP	I2C1_SDA	UART7_RX	–	–	–
49	PB2	SDC0_D3	SPI0_CS	–	–	–	–	–
50	PB3	SDC0_D0	SPI0_MISO	–	–	–	–	–
51	PB4	SDC0_D1	SPI0_MOSI	–	–	–	–	–
52	PB5	SDC0_D2	SPI0_CLK	–	–	–	–	–

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Table 5–2 D211BB (Sip DDR2) / D211BC (Sip DDR3) QFN88 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
GPIO C								
33	PC0	SDC1_D1	LCD_D5	SPI2_CLK	UART1_TX	JTAG_MS	PWM0_A	–
34	PC1	SDC1_D0	LCD_D4	SPI2_CS	UART1_RX	JTAG_DI	PWM0_B	–
35	PC2	SDC1_CLK	LCD_D3	SPI2_MOSI	UART1_RTS	UART0_TX	PWM1_A	–
36	PC3	SDC1_CMD	LCD_D2	SPI2_MISO	UART2_TX	JTAG_DO	PWM1_B	–
37	PC4	SDC1_D3	LCD_D1	–	UART2_RX	UART0_RX	PWM2_A	–
38	PC5	SDC1_D2	LCD_D0	UART2_RTS	UART3_TX	JTAG_CK	PWM2_B	–
39	PC6	SDC1_DET	CLK_OUT0	DE_TE	UART3_RX	–	PWM3_A	–
GPIO D								
32	PD6	LCD_D6	SPI3_MISO	I2C0_SCL	UART1_TX	–	–	–
31	PD7	LCD_D7	SPI2_MISO	I2C0_SDA	UART1_RX	–	–	–
30	PD8	LCD_D8	LVDS1_D0N	SPI1_HOLD	UART2_TX	–	EPWM0_A	–
29	PD9	LCD_D9	LVDS1_D0P	SPI1_WP	UART2_RX	–	EPWM0_B	–
28	PD10	LCD_D10	LVDS1_D1N	SPI1_CS0	UART3_TX	–	EPWM1_A	–
27	PD11	LCD_D11	LVDS1_D1P	SPI1_MISO	UART3_RX	–	EPWM1_B	–
26	PD12	LCD_D12	LVDS1_D2N	SPI1_MOSI	UART4_TX	–	EPWM2_A	–
25	PD13	LCD_D13	LVDS1_D2P	SPI1_CLK	UART4_RX	–	EPWM2_B	–
24	PD14	LCD_D14	LVDS1_CKN	SPI3_CLK	CAP0	–	QEP0_H0	–
23	PD15	LCD_D15	LVDS1_CKP	SPI3_CS0	CAP1	–	QEP0_H1	–
22	PD16	LCD_D16	LVDS1_D3N	SPI3_MOSI	CAP2	–	QEP0_H2	–
21	PD17	LCD_D17	LVDS1_D3P	SPI3_MISO	–	–	QEP0_A	–
19	PD18	LCD_D18	LVDS0_D0N	DSI_D0N	I2C1_SCL	–	QEP0_B	–
18	PD19	LCD_D19	LVDS0_D0P	DSI_D0P	I2C1_SDA	–	QEP0_I	–
17	PD20	LCD_D20	LVDS0_D1N	DSI_D1N	UART7_TX	–	QEP0_S	–
16	PD21	LCD_D21	LVDS0_D1P	DSI_D1P	UART7_RX	CLK_OUT0	–	–
15	PD22	LCD_D22	LVDS0_D2N	DSI_CKN	I2C3_SCL	UART6_TX	–	–
14	PD23	LCD_D23	LVDS0_D2P	DSI_CKP	I2C3_SDA	UART6_RX	–	–
13	PD24	LCD_DCLK	LVDS0_CKN	DSI_D2N	UART5_TX	SPI1_CLK	–	–
12	PD25	LCD_HS	LVDS0_CKP	DSI_D2P	UART5_RX	SPI1_CS0	–	–
11	PD26	LCD_VS	LVDS0_D3N	DSI_D3N	PWM3_A	SPI1_MOSI	–	–
10	PD27	LCD_DE	LVDS0_D3P	DSI_D3P	PWM3_B	SPI1_MISO	–	RTC_32K
GPIO E								
54	PE0	–	DVP_D0	I2C0_SCL	–	EMAC0_RXD1	EPWM3_A	PWM0_A
55	PE1	–	DVP_D1	I2C0_SDA	–	EMAC0_RXD0	EPWM3_B	PWM0_B
56	PE2	–	DVP_D2	CAN0_TX	UART4_TX	EMAC0_CRS_DV	EPWM4_A	PWM1_A
57	PE3	–	DVP_D3	CAN0_RX	UART4_RX	EMAC0_REFCLK	EPWM4_B	PWM1_B
59	PE4	–	DVP_D4	CAN1_TX	UART5_TX	EMAC0_TXD1	EPWM5_A	PWM2_A
60	PE5	–	DVP_D5	CAN1_RX	UART5_RX	EMAC0_TXD0	EPWM5_B	PWM2_B
61	PE6	DSPK0	DVP_D6	UART5_RTS	UART6_TX	EMAC0_TXC	QEP1_H0	CAP0
62	PE7	DSPK1	DVP_D7	UART7_RTS	UART6_RX	EMAC0_TXEN	QEP1_H1	CAP1
63	PE8	I2S0_MCLK	DVP_CK	UART6_RTS	UART7_TX	EMAC0_MDC	QEP1_H2	CAP2

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Table 5–2 D211BB (Sip DDR2) / D211BC (Sip DDR3) QFN88 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
64	PE9	I2S0_BCLK	DVP_HS	UART6_CTS	UART7_RX	EMAC0_MDIO	QEP1_A	–
65	PE10	I2S0_LRCK	DVP_VS	DSPK0	–	CLK_OUT2	QEP1_B	–
66	PE11	I2S0_DOUT	I2S0_DIN	DSPK1	CLK_OUT1	–	QEP1_I	–
67	PE14	–	SPI3_MOSI	–	UART3_TX	–	CAP1	–
68	PE15	–	SPI3_MISO	–	UART3_RX	–	CAP2	–
69	PE16	–	SPI0_CLK	CAN0_TX	I2C3_SCL	–	–	–
70	PE17	–	SPI0_CS	CAN0_RX	I2C3_SDA	–	–	–
71	PE18	–	SPI0_MOSI	CAN1_TX	PWM3_A	–	–	–
72	PE19	–	SPI0_MISO	CAN1_RX	PWM3_B	–	–	–
GPIO F								
5	PF0	SDC2_D1	SPI2_CLK	–	UART5_TX	–	–	–
6	PF1	SDC2_D0	SPI2_CS	–	UART5_RX	–	–	–
8	PF14	I2S1_DIN	DSPK0	DMIC_D0	UART4_TX	–	–	–
9	PF15	DE_TE	DSPK1	DMIC_CLK	UART4_RX	–	–	–
USB								
78	PU0	USB0_DM	–	UART0_RX	UART1_RX	–	–	–
79	PU1	USB0_DP	–	UART0_TX	UART1_TX	–	–	–

5.3.1.2. D211DB/ D211DC QFN100 Package Pin Description

Table 5–3 D211DB (Sip DDR2)/ D211DC (Sip DDR3) QFN100 Package Pin Description

Pins	Definition	Signal Type	Function	Remark
RTC				
74	RTC_IO	OD	RTC 32K clock output	OD output, with an external pullup resistor. The pullup voltage must be lower than 5 V.
75	RTC_VCOIN	POWER	–	Can be floating if power–off protection is not considered. The internal diode can be powered by a 3.3–V source. If connected externally for power supply, a RC must be connected for power–on delay (10 KΩ/ 0.1 uF).
76	RTC_XO	OUTPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
77	RTC_XI	INPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
SYSTEM				
58	RESETN	INPUT	System Reset	Built in with a 30 KΩ pullup resistor and dithering filter which can be floating if not used. If an external capacitor is connected, the recommended load capacitance is less than 4.7 uF.
59	PLL_XO	OUTPUT	–	Connect with a 24–MHz crystal oscillator.
60	PLL_XI	INPUT	–	Connect with a 24–MHz crystal oscillator.
POWER				
41, 65	VCC33_IO0	POWER	IO Voltage	3.3 –V power supply

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Table 5–3 D211DB (Sip DDR2)/ D211DC (Sip DDR3) QFN100 Package Pin Description (continued)

Pins	Definition	Signal Type	Function	Remark
21, 88	VCC33_IO1	POWER	IO Voltage	3.3 –V power supply
66	VCC30_ANA	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
23	LDO25	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
22	LDO1x	POWER	Built–in LDO output	Configurable. Connect with a 1–uF bypass capacitor if needed. In this case, chip cooling must be considered.
24, 26, 27, 29	VCC_DRAM	POWER	DRAW power source	DDR2 1.8 V power supplyDDR3 1.5 V power supply
1, 25, 28, 36, 56, 57	VDD11_SYS	POWER	Chip Core Voltage	1.2 V power supply @600 MHz, 1.1 V power supply @504 MHz.
101	GND	POWER	–	GND Copper full–cover connection via stitching for cooling.

Table 5–4 D211DB (Sip DDR2) / D211DC(Sip DDR3) QFN100 Package Pin–mux

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
GPIO A								
67	PA0	GPADC0	PSADC0	I2C0_SCL	UART0_TX	AMIC_IN	IR_TX	–
68	PA1	GPADC1	PSADC1	I2C0_SDA	UART0_RX	AMIC_BIAS	IR_RX	–
69	PA7	GPADC7	PSADC7	I2C1_SDA	UART1_CTS	–	–	–
70	PA8	RTP_XP	PSADC8	I2C2_SCL	UART2_TX	JTAG_DO	–	–
71	PA9	RTP_YP	PSADC9	I2C2_SDA	UART2_RX	JTAG_DI	–	–
72	PA10	RTP_XN	PSADC10	I2C3_SCL	UART2_RTS	JTAG_MS	–	–
73	PA11	RTP_YN	PSADC11	I2C3_SDA	UART2_CTS	JTAG_CK	–	–
GPIO B								
30	PB0	SDC0_CMD	SPI0_HOLD	I2C1_SCL	UART7_TX	–	–	–
31	PB1	SDC0_CLK	SPI0_WP	I2C1_SDA	UART7_RX	–	–	–
32	PB2	SDC0_D3	SPI0_CS	–	–	–	–	–
33	PB3	SDC0_D0	SPI0_MISO	–	–	–	–	–
34	PB4	SDC0_D1	SPI0_MOSI	–	–	–	–	–
35	PB5	SDC0_D2	SPI0_CLK	–	–	–	–	–
GPIO C								
14	PC0	SDC1_D1	LCD_D5	SPI2_CLK	UART1_TX	JTAG_MS	PWM0_A	–
15	PC1	SDC1_D0	LCD_D4	SPI2_CS	UART1_RX	JTAG_DI	PWM0_B	–
16	PC2	SDC1_CLK	LCD_D3	SPI2_MOSI	UART1_RTS	UART0_TX	PWM1_A	–
17	PC3	SDC1_CMD	LCD_D2	SPI2_MISO	UART2_TX	JTAG_DO	PWM1_B	–
18	PC4	SDC1_D3	LCD_D1	–	UART2_RX	UART0_RX	PWM2_A	–
19	PC5	SDC1_D2	LCD_D0	UART2_RTS	UART3_TX	JTAG_CK	PWM2_B	–
20	PC6	SDC1_DET	CLK_OUT0	DE_TE	UART3_RX	–	PWM3_A	–
GPIO D								
13	PD6	LCD_D6	SPI3_MISO	I2C0_SCL	UART1_TX	PBUS_AD6	–	–
12	PD7	LCD_D7	SPI2_MISO	I2C0_SDA	UART1_RX	PBUS_AD7	–	–
11	PD8	LCD_D8	LVDS1_D0N	SPI1_HOLD	UART2_TX	PBUS_AD8	EPWM0_A	–

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Table 5–4 D211DB (Sip DDR2) / D211DC(Sip DDR3) QFN100 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
10	PD9	LCD_D9	LVDS1_D0P	SPI1_WP	UART2_RX	PBUS_AD9	EPWM0_B	–
9	PD10	LCD_D10	LVDS1_D1N	SPI1_CS0	UART3_TX	PBUS_AD10	EPWM1_A	–
8	PD11	LCD_D11	LVDS1_D1P	SPI1_MISO	UART3_RX	PBUS_AD11	EPWM1_B	–
7	PD12	LCD_D12	LVDS1_D2N	SPI1_MOSI	UART4_TX	PBUS_AD12	EPWM2_A	–
6	PD13	LCD_D13	LVDS1_D2P	SPI1_CLK	UART4_RX	PBUS_AD13	EPWM2_B	–
5	PD14	LCD_D14	LVDS1_CKN	SPI3_CLK	CAP0	PBUS_AD14	QEP0_H0	–
4	PD15	LCD_D15	LVDS1_CKP	SPI3_CS0	CAP1	PBUS_AD15	QEP0_H1	–
3	PD16	LCD_D16	LVDS1_D3N	SPI3_MOSI	CAP2	PBUS_CLK	QEP0_H2	–
2	PD17	LCD_D17	LVDS1_D3P	SPI3_MISO	–	PBUS_NCS	QEP0_A	–
100	PD18	LCD_D18	LVDS0_D0N	DSI_D0N	I2C1_SCL	PBUS_NADV	QEP0_B	–
99	PD19	LCD_D19	LVDS0_D0P	DSI_D0P	I2C1_SDA	PBUS_NWE	QEP0_I	–
98	PD20	LCD_D20	LVDS0_D1N	DSI_D1N	UART7_TX	PBUS_NOE	QEP0_S	–
97	PD21	LCD_D21	LVDS0_D1P	DSI_D1P	UART7_RX	CLK_OUT0	–	–
96	PD22	LCD_D22	LVDS0_D2N	DSI_CKN	I2C3_SCL	UART6_TX	–	–
95	PD23	LCD_D23	LVDS0_D2P	DSI_CKP	I2C3_SDA	UART6_RX	–	–
94	PD24	LCD_DCLK	LVDS0_CKN	DSI_D2N	UART5_TX	SPI1_CLK	–	–
93	PD25	LCD_HS	LVDS0_CKP	DSI_D2P	UART5_RX	SPI1_CS0	–	–
92	PD26	LCD_VS	LVDS0_D3N	DSI_D3N	PWM3_A	SPI1_MOSI	–	–
91	PD27	LCD_DE	LVDS0_D3P	DSI_D3P	PWM3_B	SPI1_MISO	–	RTC_32K
GPIO E								
37	PE0	–	DVP_D0	I2C0_SCL	–	EMAC0_RXD1	EPWM3_A	PWM0_A
38	PE1	–	DVP_D1	I2C0_SDA	–	EMAC0_RXD0	EPWM3_B	PWM0_B
39	PE2	–	DVP_D2	CAN0_TX	UART4_TX	EMAC0_CRS_DV	EPWM4_A	PWM1_A
40	PE3	–	DVP_D3	CAN0_RX	UART4_RX	EMAC0_REFCLK	EPWM4_B	PWM1_B
42	PE4	–	DVP_D4	CAN1_TX	UART5_TX	EMAC0_TXD1	EPWM5_A	PWM2_A
43	PE5	–	DVP_D5	CAN1_RX	UART5_RX	EMAC0_TXD0	EPWM5_B	PWM2_B
44	PE6	DSPK0	DVP_D6	UART5_RTS	UART6_TX	EMAC0_TXC	QEP1_H0	CAP0
45	PE7	DSPK1	DVP_D7	UART7_RTS	UART6_RX	EMAC0_TXEN	QEP1_H1	CAP1
46	PE8	I2S0_MCLK	DVP_CK	UART6_RTS	UART7_TX	EMAC0_MDC	QEP1_H2	CAP2
47	PE9	I2S0_BCLK	DVP_HS	UART6_CTS	UART7_RX	EMAC0_MDIO	QEP1_A	–
48	PE10	I2S0_LRCK	DVP_VS	DSPK0	–	CLK_OUT2	QEP1_B	–
49	PE11	I2S0_DOUT	I2S0_DIN	DSPK1	CLK_OUT1	–	QEP1_I	–
50	PE14	–	SPI3_MOSI	–	UART3_TX	–	CAP1	–
51	PE15	–	SPI3_MISO	–	UART3_RX	–	CAP2	–
52	PE16	–	SPI0_CLK	CAN0_TX	I2C3_SCL	–	–	–
53	PE17	–	SPI0_CS	CAN0_RX	I2C3_SDA	–	–	–
54	PE18	–	SPI0_MOSI	CAN1_TX	PWM3_A	–	–	–
55	PE19	–	SPI0_MISO	CAN1_RX	PWM3_B	–	–	–
GPIO F								
78	PF0	SDC2_D1	SPI2_CLK	–	UART5_TX	EMAC1_RXD1	PBUS_AD0	–
79	PF1	SDC2_D0	SPI2_CS	–	UART5_RX	EMAC1_RXD0	PBUS_AD1	–

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Table 5–4 D211DB (Sip DDR2) / D211DC(Sip DDR3) QFN100 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
80	PF2	SDC2_CLK	SPI2_MOSI	–	UART5_RTS	EMAC1_CRS_DV	PBUS_AD2	–
81	PF3	SDC2_CMD	SPI2_MISO	–	UART5_CTS	EMAC1_REFCLK	PBUS_AD3	–
82	PF4	SDC2_D3	–	–	UART6_TX	EMAC1_TXD1	PBUS_AD4	–
83	PF5	SDC2_D2	–	–	UART6_RX	EMAC1_TXD0	PBUS_AD5	–
84	PF6	–	–	–	UART7_TX	EMAC1_TXC	PBUS_AD6	–
85	PF7	–	–	–	UART7_RX	EMAC1_TXEN	PBUS_AD7	–
86	PF8	–	–	–	UART7_RTS	EMAC1_MDC	PBUS_AD8	–
87	PF9	–	–	–	UART7_CTS	EMAC1_MDIO	PBUS_AD9	–
89	PF14	I2S1_DIN	DSPK0	DMIC_D0	UART4_TX	–	PBUS_NWE	–
90	PF15	DE_TE	DSPK1	DMIC_CLK	UART4_RX	–	PBUS_NOE	–
USB								
61	PU0	USB0_DM	–	UART0_RX	UART1_RX	–	–	–
62	PU1	USB0_DP	–	UART0_TX	UART1_TX	–	–	–
63	PU2	USB1_DM	–	UART0_RX	UART2_RX	–	–	–
64	PU3	USB1_DP	–	UART0_TX	UART2_TX	–	–	–

5.3.1.3. D213EC QFN128 Package Pin Description

Table 5–5 D213EC (Sip DDR3) QFN128 Package Pin Description

Pins	Definition	Signal Type	Function	Remark
RTC				
97	RTC_IO	OD	RTC 32K clock output	OD output, with an external pullup resistor. The pullup voltage must be lower than 5 V.
98	RTC_VCOIN	POWER	–	Can be floating if power–off protection is not considered. The internal diode can be powered by a 3.3–V source. If connected externally for power supply, a RC must be connected for power–on delay (10 KΩ/ 0.1 uF).
99	RTC_XO	OUTPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
100	RTC_XI	INPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
SYSTEM				
76	RESETN	INPUT	System Reset	Built in with a 30kΩ pullup resistor and dithering filter which can be floating if not used. If an external capacitor is connected, the recommended load capacitance is less than 4.7 uF.
77	PLL_XO	OUTPUT	–	Connect with a 24–MHz crystal oscillator.
78	PLL_XI	INPUT	–	Connect with a 24–MHz crystal oscillator.
POWER				
41, 57, 83	VCC33_IO0	POWER	IO Voltage	3.3 –V power supply
27, 114	VCC33_IO1	POWER	IO Voltage	3.3 –V power supply
84	VCC30_ANA	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor

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Table 5–5 D213EC (Sip DDR3) QFN128 Package Pin Description (continued)

Pins	Definition	Signal Type	Function	Remark
29	LDO25	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
28	LDO1x	POWER	Built–in LDO output	Configurable. Connect with a 1–uF bypass capacitor if needed. In this case, chip cooling must be considered.
30, 32, 33, 35, 36	VCC_DRAM	POWER	DRAW power source	DDR2 1.8 V power supplyDDR3 1.5 V power supply
31, 34, 44, 74, 75, 128	VDD11_SYS	POWER	Chip Core Voltage	1.2 V power supply @600 MHz, 1.1 V power supply @504 MHz.
129	GND	POWER	–	GND Copper full–cover connection via stitching for cooling.
50, 56	NC	–	–	floating input with no signal.

Table 5–6 D213EC (Sip DDR3) QFN128 Package Pin–mux

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
GPIO A								
85	PA0	GPADC0	PSADC0	I2C0_SCL	UART0_TX	AMIC_IN	IR_TX	–
86	PA1	GPADC1	PSADC1	I2C0_SDA	UART0_RX	AMIC_BIAS	IR_RX	–
87	PA2	GPADC2	PSADC2	–	UART0_RTS	–	–	–
88	PA3	GPADC3	PSADC3	–	UART0_CTS	–	–	–
89	PA4	GPADC4	PSADC4	–	UART1_TX	–	–	–
90	PA5	GPADC5	PSADC5	–	UART1_RX	–	–	–
91	PA6	GPADC6	PSADC6	I2C1_SCL	UART1_RTS	–	–	–
92	PA7	GPADC7	PSADC7	I2C1_SDA	UART1_CTS	–	–	–
93	PA8	RTP_XP	PSADC8	I2C2_SCL	UART2_TX	JTAG_DO	–	–
94	PA9	RTP_YP	PSADC9	I2C2_SDA	UART2_RX	JTAG_DI	–	–
95	PA10	RTP_XN	PSADC10	I2C3_SCL	UART2_RTS	JTAG_MS	–	–
96	PA11	RTP_YN	PSADC11	I2C3_SDA	UART2_CTS	JTAG_CK	–	–
GPIO B								
37	PB0	SDC0_CMD	SPI0_HOLD	I2C1_SCL	UART7_TX	–	–	–
38	PB1	SDC0_CLK	SPI0_WP	I2C1_SDA	UART7_RX	–	–	–
39	PB2	SDC0_D3	SPI0_CS	–	–	–	–	–
40	PB3	SDC0_D0	SPI0_MISO	–	–	–	–	–
42	PB4	SDC0_D1	SPI0_MOSI	–	–	–	–	–
43	PB5	SDC0_D2	SPI0_CLK	–	–	–	–	–
45	PB6	SDC0_D4	SPI1_HOLD	I2C2_SCL	UART4_TX	–	CLK_OUT2	–
46	PB7	SDC0_D5	SPI1_WP	I2C2_SDA	UART4_RX	–	–	–
47	PB8	SDC0_D6	SPI1_CS0	UART4_RTS	UART5_TX	–	IR_RX	–
48	PB9	SDC0_D7	SPI1_MISO	UART6_RTS	UART5_RX	–	IR_TX	–
49	PB10	SDC0_DS	SPI1_MOSI	–	UART6_TX	–	–	–
51	PB11	SDC0_RST	SPI1_CLK	–	UART6_RX	–	–	–
GPIO C								
19	PC0	SDC1_D1	LCD_D5	SPI2_CLK	UART1_TX	JTAG_MS	PWM0_A	–

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Table 5–6 D213EC (Sip DDR3) QFN128 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
20	PC1	SDC1_D0	LCD_D4	SPI2_CS	UART1_RX	JTAG_DI	PWM0_B	–
21	PC2	SDC1_CLK	LCD_D3	SPI2_MOSI	UART1_RTS	UART0_TX	PWM1_A	–
22	PC3	SDC1_CMD	LCD_D2	SPI2_MISO	UART2_TX	JTAG_DO	PWM1_B	–
23	PC4	SDC1_D3	LCD_D1	–	UART2_RX	UART0_RX	PWM2_A	–
24	PC5	SDC1_D2	LCD_D0	UART2_RTS	UART3_TX	JTAG_CK	PWM2_B	–
25	PC6	SDC1_DET	CLK_OUT0	DE_TE	UART3_RX	–	PWM3_A	–
26	PC7	–	–	–	UART3_RTS	–	PWM3_B	–
GPIO D								
18	PD0	LCD_D0	SPI2_CLK	–	–	PBUS_AD0	PWM0_A	–
17	PD1	LCD_D1	SPI2_CS	–	–	PBUS_AD1	PWM0_B	–
16	PD2	LCD_D2	SPI2_MOSI	DE_TE	–	PBUS_AD2	PWM1_A	–
15	PD3	LCD_D3	SPI3_CLK	–	–	PBUS_AD3	PWM1_B	–
14	PD4	LCD_D4	SPI3_CS0	–	–	PBUS_AD4	PWM2_A	–
13	PD5	LCD_D5	SPI3_MOSI	–	–	PBUS_AD5	PWM2_B	–
12	PD6	LCD_D6	SPI3_MISO	I2C0_SCL	UART1_TX	PBUS_AD6	–	–
11	PD7	LCD_D7	SPI2_MISO	I2C0_SDA	UART1_RX	PBUS_AD7	–	–
10	PD8	LCD_D8	LVDS1_D0N	SPI1_HOLD	UART2_TX	PBUS_AD8	EPWM0_A	–
9	PD9	LCD_D9	LVDS1_D0P	SPI1_WP	UART2_RX	PBUS_AD9	EPWM0_B	–
8	PD10	LCD_D10	LVDS1_D1N	SPI1_CS0	UART3_TX	PBUS_AD10	EPWM1_A	–
7	PD11	LCD_D11	LVDS1_D1P	SPI1_MISO	UART3_RX	PBUS_AD11	EPWM1_B	–
6	PD12	LCD_D12	LVDS1_D2N	SPI1_MOSI	UART4_TX	PBUS_AD12	EPWM2_A	–
5	PD13	LCD_D13	LVDS1_D2P	SPI1_CLK	UART4_RX	PBUS_AD13	EPWM2_B	–
4	PD14	LCD_D14	LVDS1_CKN	SPI3_CLK	CAP0	PBUS_AD14	QEP0_H0	–
3	PD15	LCD_D15	LVDS1_CKP	SPI3_CS0	CAP1	PBUS_AD15	QEP0_H1	–
2	PD16	LCD_D16	LVDS1_D3N	SPI3_MOSI	CAP2	PBUS_CLK	QEP0_H2	–
1	PD17	LCD_D17	LVDS1_D3P	SPI3_MISO	–	PBUS_NCS	QEP0_A	–
127	PD18	LCD_D18	LVDS0_D0N	DSI_D0N	I2C1_SCL	PBUS_NADV	QEP0_B	–
126	PD19	LCD_D19	LVDS0_D0P	DSI_D0P	I2C1_SDA	PBUS_NWE	QEP0_I	–
125	PD20	LCD_D20	LVDS0_D1N	DSI_D1N	UART7_TX	PBUS_NOE	QEP0_S	–
124	PD21	LCD_D21	LVDS0_D1P	DSI_D1P	UART7_RX	CLK_OUT0	–	–
123	PD22	LCD_D22	LVDS0_D2N	DSI_CKN	I2C3_SCL	UART6_TX	–	–
122	PD23	LCD_D23	LVDS0_D2P	DSI_CKP	I2C3_SDA	UART6_RX	–	–
121	PD24	LCD_DCLK	LVDS0_CKN	DSI_D2N	UART5_TX	SPI1_CLK	–	–
120	PD25	LCD_HS	LVDS0_CKP	DSI_D2P	UART5_RX	SPI1_CS0	–	–
119	PD26	LCD_VS	LVDS0_D3N	DSI_D3N	PWM3_A	SPI1_MOSI	–	–
118	PD27	LCD_DE	LVDS0_D3P	DSI_D3P	PWM3_B	SPI1_MISO	–	RTC_32K
GPIO E								
52	PE0	–	DVP_D0	I2C0_SCL	–	GMAC0_RXD1	EPWM3_A	PWM0_A
53	PE1	–	DVP_D1	I2C0_SDA	–	GMAC0_RXD0	EPWM3_B	PWM0_B
54	PE2	–	DVP_D2	CAN0_TX	UART4_TX	GMAC0_RXCTL	EPWM4_A	PWM1_A
55	PE3	–	DVP_D3	CAN0_RX	UART4_RX	GMAC0_CLKIN	EPWM4_B	PWM1_B

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Table 5–6 D213EC (Sip DDR3) QFN128 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
58	PE4	–	DVP_D4	CAN1_TX	UART5_TX	GMAC0_TXD1	EPWM5_A	PWM2_A
59	PE5	–	DVP_D5	CAN1_RX	UART5_RX	GMAC0_TXD0	EPWM5_B	PWM2_B
60	PE6	DSPK0	DVP_D6	UART5_RTS	UART6_TX	GMAC0_TXCK	QEP1_H0	CAP0
61	PE7	DSPK1	DVP_D7	UART7_RTS	UART6_RX	GMAC0_TXCTL	QEP1_H1	CAP1
62	PE8	I2S0_MCLK	DVP_CK	UART6_RTS	UART7_TX	GMAC0_MDC	QEP1_H2	CAP2
63	PE9	I2S0_BCLK	DVP_HS	UART6_CTS	UART7_RX	GMAC0_MDIO	QEP1_A	–
64	PE10	I2S0_LRCK	DVP_VS	DSPK0	–	CLK_OUT2	QEP1_B	–
65	PE11	I2S0_DOUT	I2S0_DIN	DSPK1	CLK_OUT1	GMAC0_RXD3	QEP1_I	–
66	PE12	I2S0_DIN	SPI3_CLK	DMIC_CLK	I2C2_SCL	GMAC0_RXD2	QEP1_S	–
67	PE13	–	SPI3_CS0	DMIC_D0	I2C2_SDA	GMAC0_RXCK	CAP0	–
68	PE14	–	SPI3_MOSI	–	UART3_TX	GMAC0_TXD3	CAP1	–
69	PE15	–	SPI3_MISO	–	UART3_RX	GMAC0_TXD2	CAP2	–
70	PE16	–	SPI0_CLK	CAN0_TX	I2C3_SCL	GMAC0_TRIG	–	–
71	PE17	–	SPI0_CS	CAN0_RX	I2C3_SDA	GMAC0_PPSO	–	–
72	PE18	–	SPI0_MOSI	CAN1_TX	PWM3_A	GMAC1_TRIG	–	–
73	PE19	–	SPI0_MISO	CAN1_RX	PWM3_B	GMAC1_PPSO	–	–
GPIO F								
101	PF0	SDC2_D1	SPI2_CLK	–	UART5_TX	GMAC1_RXD1	PBUS_AD0	–
102	PF1	SDC2_D0	SPI2_CS	–	UART5_RX	GMAC1_RXD0	PBUS_AD1	–
103	PF2	SDC2_CLK	SPI2_MOSI	–	UART5_RTS	GMAC1_RXCTL	PBUS_AD2	–
104	PF3	SDC2_CMD	SPI2_MISO	–	UART5_CTS	GMAC1_CLKIN	PBUS_AD3	–
105	PF4	SDC2_D3	–	–	UART6_TX	GMAC1_TXD1	PBUS_AD4	–
106	PF5	SDC2_D2	–	–	UART6_RX	GMAC1_TXD0	PBUS_AD5	–
107	PF6	–	–	–	UART7_TX	GMAC1_TXCK	PBUS_AD6	–
108	PF7	–	–	–	UART7_RX	GMAC1_TXCTL	PBUS_AD7	–
109	PF8	–	–	–	UART7_RTS	GMAC1_MDC	PBUS_AD8	–
110	PF9	–	–	–	UART7_CTS	GMAC1_MDIO	PBUS_AD9	–
111	PF10	I2S1_MCLK	I2S1_DIN	–	UART3_CTS	CLK_OUT3	PBUS_AD10	–
112	PF11	I2S1_BCLK	–	PBUS_AD11	UART3_TX	GMAC1_RXD3	PBUS_CLK	–
113	PF12	I2S1_LRCK	–	UART4_RTS	UART3_RX	GMAC1_RXD2	PBUS_NCS	–
115	PF13	I2S1_DOUT	I2S1_DIN	UART4_CTS	UART3_RTS	GMAC1_RXCK	PBUS_NADV	–
116	PF14	I2S1_DIN	DSPK0	DMIC_D0	UART4_TX	GMAC1_TXD3	PBUS_NWE	–
117	PF15	DE_TE	DSPK1	DMIC_CLK	UART4_RX	GMAC1_TXD2	PBUS_NOE	–
USB								
79	PU0	USB0_DM	–	UART0_RX	UART1_RX	–	–	–
80	PU1	USB0_DP	–	UART0_TX	UART1_TX	–	–	–
81	PU2	USB1_DM	–	UART0_RX	UART2_RX	–	–	–
82	PU3	USB1_DP	–	UART0_TX	UART2_TX	–	–	–

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5.4. Pin Description

Pin/Signal Name	Description	Signal Type
SYSTEM		
RESET	Reset pin	I
PLL_XI	24 –MHz crystal oscillator input capacitance	AI
PLL_XO	24 MHz crystal oscillator	AO
RTC		
RTC_IO	RTC wakeup output	OD
RTC_VCOIN	Button–cell power source for RTC	P
RTC_XO	32.768 KHz crystal oscillator	AO
RTC_XI	32.768 –KHz crystal oscillator input capacitance	AI
USB		
USB0_DM	USB0 Data Minus	AI/O
USB0_DP	USB0 Data Positive	AI/O
USB1_DM	USB1 Data Minus	AI/O
USB1_DP	USB1 Data Positive	AI/O
RTP		
RTP_XP	RTP X positive	AI
RTP_YP	RTP Y positive	AI
RTP_XN	RTP X negative	AI
RTP_YN	RTP Y negative	AI
ADC，x = 0~7		
GPADCx	General–purpose analog input	AI
ADC，x = 0~11		
PSADCx	General–purpose analog input	AI
AMIC		
AMIC_IN	Analog microphone input	AI
AMIC_BIAS	Analog microphone bias	AO
EMAC，x = 0~1		
EMACx_RXD1	RMII receive data 1	I
EMACx_RXD0	RMII receive data 0	I
EMACx_CRS_DV	RMII receive data valid	I
EMACx_REFCLK	RMII reference clock	I
EMACx_TXD1	RMII transmit data 1	O
EMACx_TXD0	RMII transmit data 0	O
EMACx_TXC	RMII transmit clock	O
EMACx_TXEN	RMII transmit enable	O
EMACx_MDC	RMII management data clock	I/O
EMACx_MDIO	RMII management data input/output	I/O
CLK_OUTx	For configuration of 25MHz clock output, x = 0~3	O
GMAC，x = 0~1		
GMACx_RXD3	RGMII receive data 3	I

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Pin/Signal Name	Description	Signal Type
GMACx_RXD2	RGMII receive data 2	I
GMACx_RXD1	RGMII receive data 1	I
GMACx_RXD0	RGMII receive data 0	I
GMACx_RXCTL	RGMII receive data control	I
GMACx_CLKIN	RGMII reference clock	I
GMACx_TXD3	RMII transmit data 3	O
GMACx_TXD2	RMII transmit data 2	O
GMACx_TXD1	RMII transmit data 1	O
GMACx_TXD0	RMII transmit data 0	O
GMACx_TXCK	RMII transmit clock	O
GMACx_TXCTL	RMII transmit data control	O
GMACx_MDC	RMII management data clock	I/O
GMACx_MDIO	RMII management data input/output	I/O
PWM，x = 0~3		
PWMx_A	PWMx Channel A	O
PWMx_B	PWMx Channel B	O
EPWM，x = 0~5		
EPWMx_A	EPWMx Channel A	O
EPWMx_B	EPWMx Channel B	O
CAP，x = 0~2		
CAPx	CAP input capture or PWM output	I/O
QEP，x = 0~1		
QEPn_A	QEPn A input signal	I
QEPn_B	QEPn B input signal	I
QEPn_I	QEPn I input/output signal	I/O
QEPn_S	QEPn S input/output signal	I/O
QEPn_H0	QEPn A Hall input signal	I
QEPn_H1	QEPn B Hall input signal	I
QEPn_H2	QEPn C Hall input signal	I
SPI，x = 0~3		
SPIx_HOLD	SPIx hold signal, valid for low-level voltage	I/O
SPIx_WP	SPIx write protection, valid for low-level voltage	I/O
SPIx_CS	SPIx chip select signal, valid for low-level voltage.	I/O
SPIx_CLK	SPIx clock signal	I/O
SPIx_MOSI	SPIx master out slave in	I/O
SPIx_MISO	SPIx master in slave out	I/O
UART，x = 0~7		
UARTx_TX	UARTx data transmission	O
UARTx_RX	UARTx data reception	I
UARTx_CTS	UARTx confirmed transmission	I
UARTx_RTS	UARTx requested transmission	O
I2C，x = 0~3		

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Pin/Signal Name	Description	Signal Type
I2Cx_SCL	I2C serial clock line	I/O
I2Cx_SDA	I2Cx serial data line	I/O
CIR		
IR_TX	Infrared data transmit	O
IR_RX	Infrared data receive	I
I2S，x = 0~1		
I2Sx_MCLK	I2Sx master clock	O
I2Sx_LRCK	I2Sx left/right clock	I/O
I2Sx_BCLK	I2Sx bit clock	I/O
I2Sx_DOUT	I2Sx data output	O
I2Sx_DIN	I2Sx data input	I
DSPK		
DSPK0	Speaker signal output channel 0	O
DSPK1	Speaker signal output channel 1	O
DMIC		
DMIC_CLK	PDM clock signal	O
DMIC_D0	PDM data signal	I/O
SDC，x = 0~2		
SDCx_CMD	SDC0 command signal	I/O
SDCx_CLK	SDC0 clock signal	O
SDCx_D[3:0]	SDC0 data output/input	I/O
LCD		
LCD_D[23:0]	LCD data output	O
LCD_DCLK	LCD clock data signal	O
LCD_HS	LCD horizontal synchronization	O
LCD_VS	LCD vertical synchronization	O
LCD_DE	LCD data enable	O
LVDS，x = 0~1		
LVDSx_CKN	LVDSx clock negative	AO
LVDSx_CKP	LVDSx clock positive	AO
LVDSx_D0N	LVDSx data 0 negative	AO
LVDSx_D0P	LVDSx data 0 positive	AO
LVDSx_D1N	LVDSx data 1 negative	AO
LVDSx_D1P	LVDSx data 1 positive	AO
LVDSx_D2N	LVDSx data 2 negative	AO
LVDSx_D2P	LVDSx data 2 positive	AO
LVDSx_D3N	LVDSx data 3 negative	AO
LVDSx_D3P	LVDSx data 3 positive	AO
MIPI DSI		
DSI_CKN	MIPI DSI clock negative	AO
DSI_CKP	MIPI DSI clock positive	AO
DSI_D0N	MIPI DSI data 0 negative	AO

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Pin/Signal Name	Description	Signal Type
DSI_D0P	MIPI DSI data 0 positive	AO
DSI_D1N	MIPI DSI data 1 negative	AO
DSI_D1P	MIPI DSI data 1 positive	AO
DSI_D2N	MIPI DSI data 2 negative	AO
DSI_D2P	MIPI DSI data 2 positive	AO
DSI_D3N	MIPI DSI data 3 negative	AO
DSI_D3P	MIPI DSI data 3 positive	AO
DVP		
DVP_CK	DVP clock	I
DVP_HS	DVP	I
DVP_VS	DVP vertical synchronization	I
DVP_D[7:0]	DVP data input	I
PBUS		
PBUS_CLK	PBUS external clock signal	O
PBUS_NCS	PBUS chip select signal, valid for low-level voltage	O
PBUS_NADV	PBUS address valid signal, valid for low-level voltage	O
PBUS_NWE	PBUS read/ write control signal, low-level voltage for write, high-level voltage for read.	O
PBUS_NOE	PBUS output enabling signal, valid for low-level voltage	O
PBUS_AD[15:0]	PBUS Address/Data Bus	I/O

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5.5. Package Size

5.5.1. D211BB / D211BC QFN88

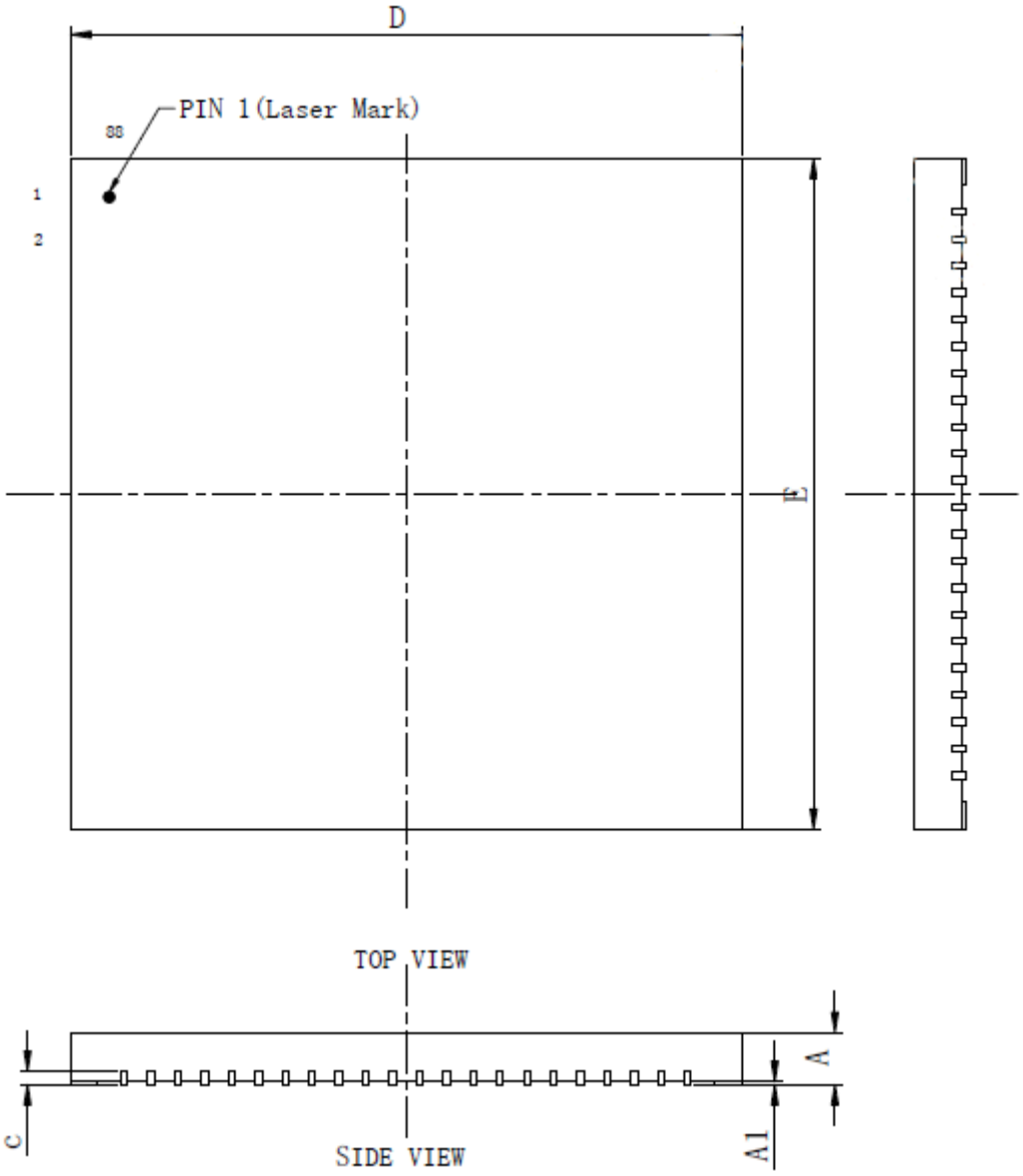

Figure 5–1 QFN88 Packaging TOP

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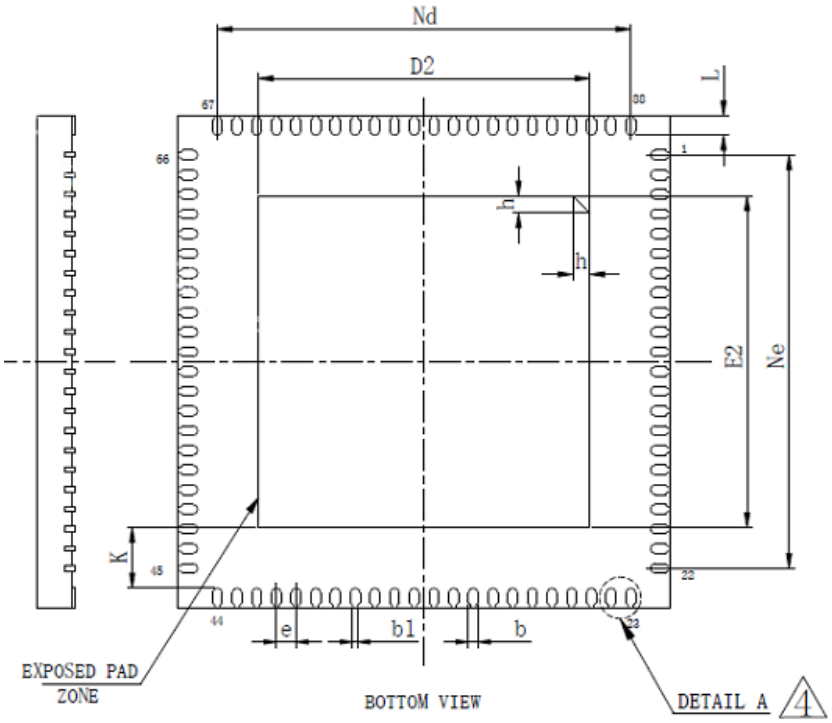

SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	1
	0.80	0.85	0.90	
	0.85	0.90	0.95	2
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.10REF			2
c	0.18	0.20	0.25	
D	9.90	10.00	10.10	
D2	6.64	6.74	6.84	
e	0.40BSC			
Nd	8.40REF			
E	9.90	10.00	10.10	
E2	6.64	6.74	6.84	
Ne	8.40REF			
L	0.30	0.40	0.50	
K	0.20	–	–	
h	0.30	0.35	0.40	

Figure 5–2 QFN88 Packaging BOTTOM

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5.5.2. D211DB / D211DC QFN100

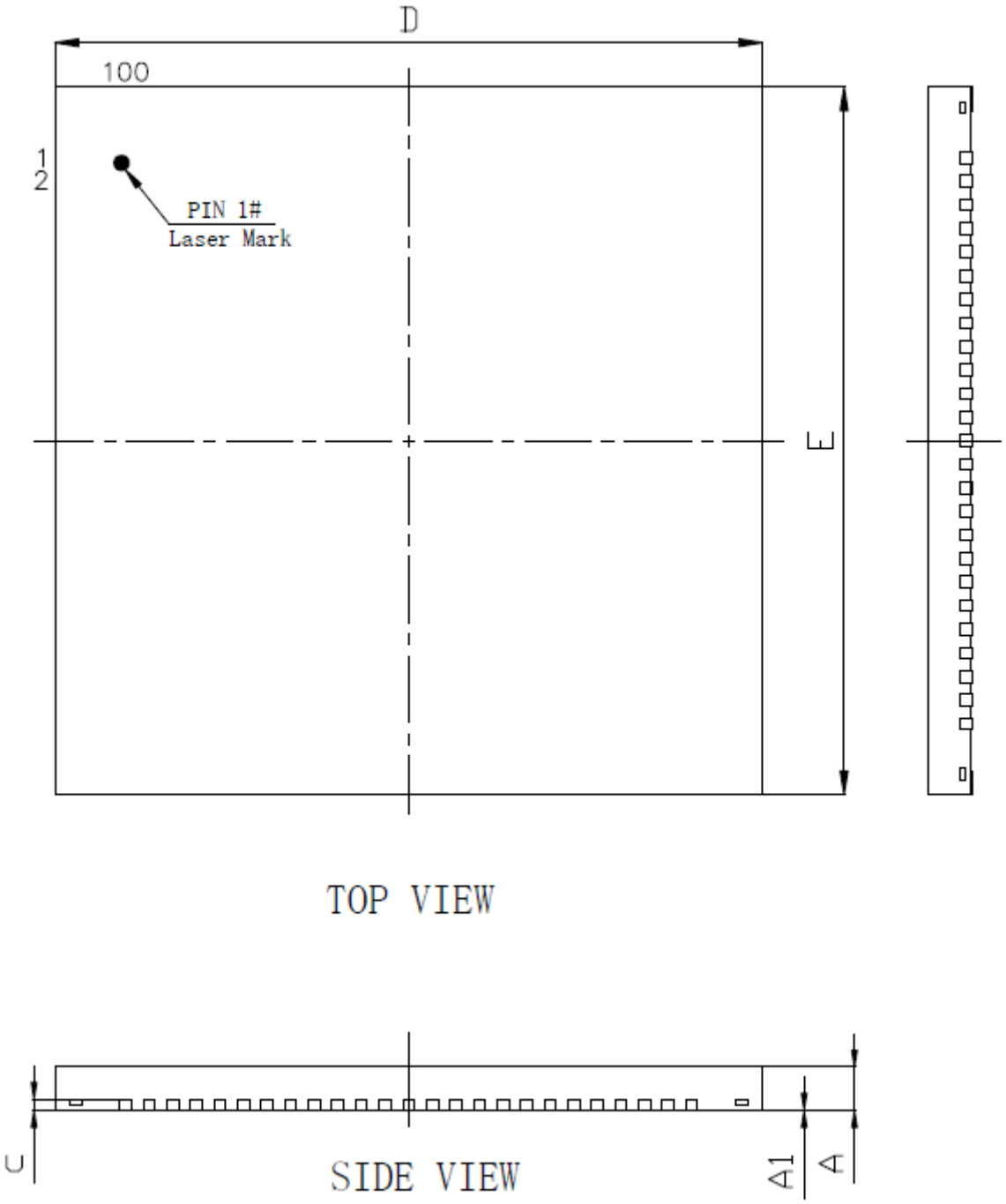

Figure 5–3 QFN100 Packaging TOP

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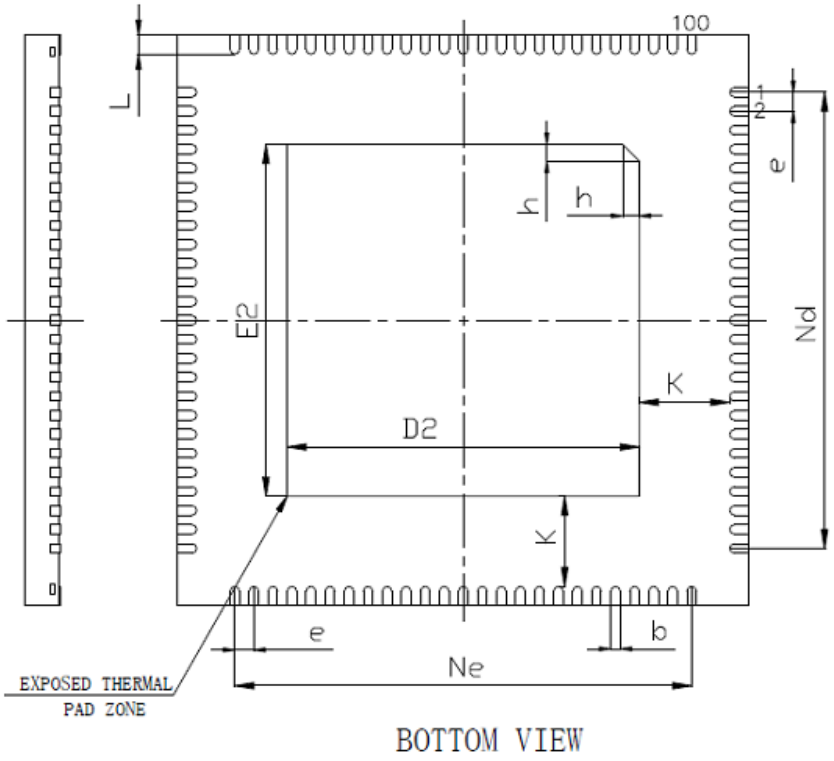

SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.80	0.85	0.90	△
	0.70	0.75	0.80	
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
c	0.203REF			
D	11.90	12.00	12.10	
D2	7.30	7.40	7.50	
e	0.40BSC			
Ne	9.60BSC			
Nd	9.60BSC			
E	11.90	12.00	12.10	
E2	7.30	7.40	7.50	
L	0.35	0.40	0.45	
h	0.30	0.35	0.40	
K	1.90REF			

Figure 5–4 QFN100 Packaging BOTTOM

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5.5.3. D213EC QFN128

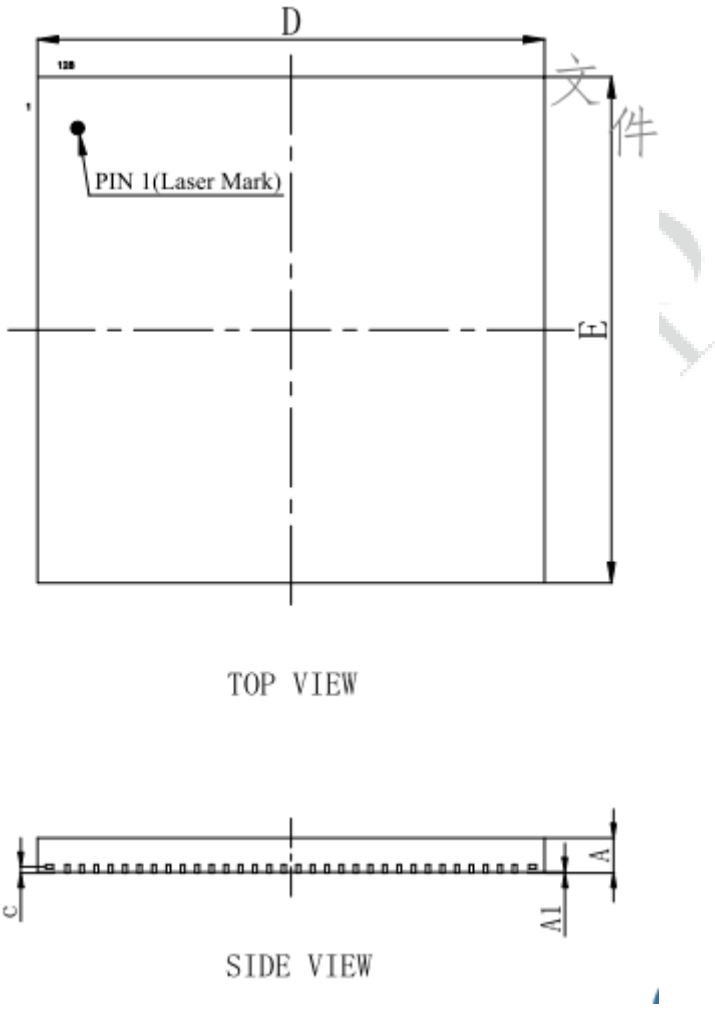
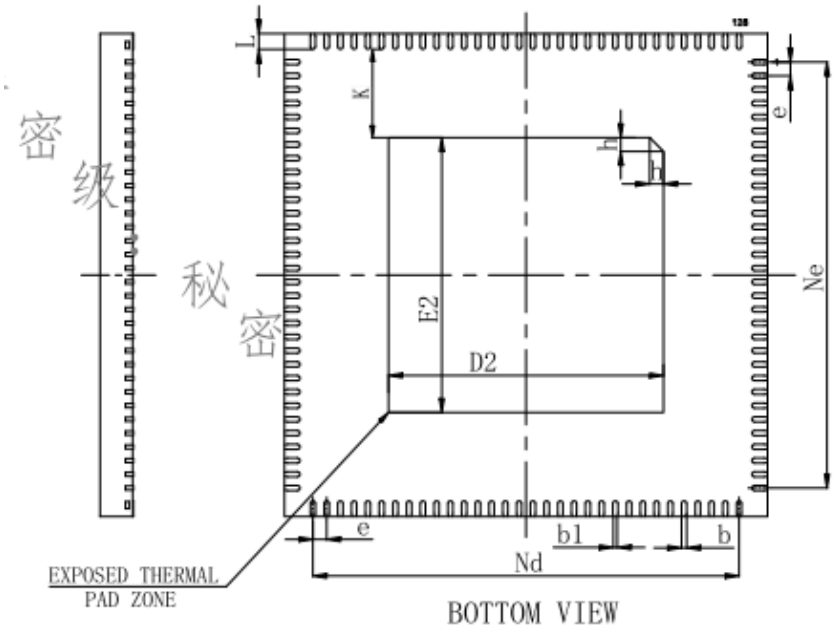


Figure 5–5 QFN128 Packaging TOP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.08	0.13	0.18
b1		0.10REF	
c		0.152REF	
D	12.20	12.30	12.40
D2	6.90	7.00	7.10
e		0.35BSC	
Nd		10.85BSC	
E	12.20	12.30	12.40
E2	6.90	7.00	7.10
Ne		10.85BSC	
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K		2.25REF	

Figure 5–6 QFN128 Packaging BOTTOM

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