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D13x Datasheet

Version 2.0

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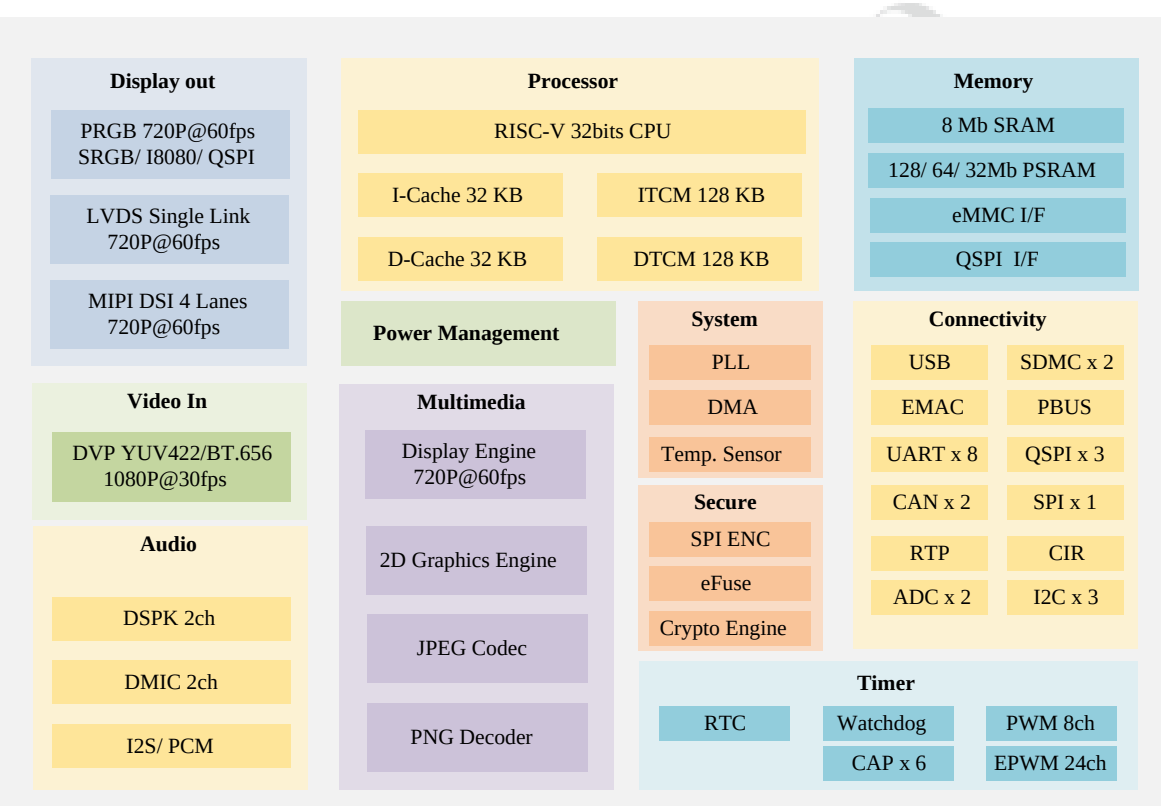
Revision History

Version	Section	Description
V1.8	–	Aligned styles.
	Functional Features	Modified function features.
	Product Information	Modified the product comparison table, and added product descriptions for D133CCS、D133ECS Sip 16–MB PSRAM.
	Electrical Features	• Modified the minimum value for RTC_VCOIN in the operating conditions. • Changed the electrical descriptions for built–in LDO.
V1.9	Power–on/Power–off Sequence and Reset	Added the following description: • The rising edge working at 3.3V shall be detected after 150 us. • The RTC_VCOIN (Real–Time Clock Voltage Input) requires an RC–delayed power–up circuit.
V2.0	Product Information	Added the following changes: • Deleted D133BAS and D132ENS. • Disabled CAN interface in D133BBS.

1. Introduction

D13x is a domestically independent MCU family based on RISC-V with high performance, industrial full-HD and smart control. Equipped with a powerful 2D image accelerator, PNG decoder, JPEG decoder engine and various display interfaces, as well as providing wide industrial temperatures, D13x is of high reliability and openness. It can be widely applied in HMI, gateways, serial display screens, smart home devices, and other pan-industrial sectors.



2. Functional Features

- **CPU Core**
  - E907 single–core processor, RV32IMAFDCP instruction set, 480 MHz@1.1V
  - 32–KB L1 instruction cache and 32 KB L1 data cache
  - Single/ double–precision floating–point unit (FPU), integrated with DSP instruction set
  - Physical Memory Protection
  - Standard CLINT and PLIC interrupt controllers
  - Machine and User Mode
  - Standard 2–wire JTAG debug interface
- **Boot**
  - Default boot sequence: SD Card(SDMC1) → SPI NOR → SPI NAND →eMMC(SDMC0)
  - Default boot device configuration available by burning eFuse
- **System Safety**
  - Secure boot by digital signatures
  - Crypto Engine (CE) with support for AES/ TDES/ RSA and SHA/ HMAC
  - SPI NAND/SPI NOR decode algorithms for SPI ENC
  - The built–in eFuse one–time programmable memory has 2048 bits, of which 512 bits are available for customer customization. It has an independent CHIPID and supports CE security key functions such as SSK/HUK/PNK/PSK0/ PSK1/PSK2/PSK3. It also supports setting read and write prohibitions.
  - Embedded 256–bit TRNG
- **On-chip Memory**
  - 64 –KB BROM
  - 1–MB SRAM, of which 256 KB can be configured for TCM
  - PSRAM has the following specification choices:
    - 128 Mb DDR, with a 16–bit bus width and a maximum frequency of 200 MHz
    - 64 Mb DDR, with a 16–bit bus width and a maximum frequency of 200 MHz
    - 32 Mb, 8–bit width, with up to 200–MHz DDR
  - Spread spectrum supported for PSRAM clock
- **Memory Interfaces**
  - SPI NAND Flash / SPI NOR Flash supported for QSPI
    - Standard, dual SPI and quad SPI supported
    - Up to 100–MHz SDR for IO
  - Two sets of eMMC 4.41/ SD 3.01/ SDIO 3.0
    - 4–bit SDR25/ SDR50/ DDR50 data transfer for eMMC
    - SDR25/ SDR50 supported for SD cards
    - Up to 50–MHz of DDR for IO with 3.3 V voltage support only
- **Graph Engine**
  - Disply Engine (DE)
    - One UI layer and one VI layer with the highest performance of 720P@60fps
    - 1/31.999x ~ 32x scaling support for VI layer
    - Dithering, Gamma and Color Correction Matrix adjustable
  - Graph Engine
    - 2D image acceleration, with a performance of up to 1080P@60fps
    - Horizontal and vertical flip support with 90/180/270–degree rotation angles
    - Rotation at any angle and scan order support for RGB graphs
    - 1/16x ~ 16x scaling scope support and 6x4–tap 16–phase filtering algorithm
    - Command queue
  - VE CODEC

- MJEPG decoder with the highest performance of 720P@60fps
- PNG decoder, with the highest performance of 720P@60fps
- JPEG decoder, with the highest performance of 720P@60fps

- **Display Interfaces**
  - 24–bit parallel port RGB, with the highest performance of 720P@60fps
  - Single Link LVDS with up to 700 Mbps of IO rate and 720P@60fps of performance
  - 1/ 2/ 4–LANE MIPI DSI with up to 1 Gbps of IO rate and 720P@60fps of performance
  - SRGB/ I8080/ QSPI interfaces
  - 8–bit DVP with up to 150 MHz of IO rate and 1080P@30fps of performance
  - Spread spectrum
- **Audio Interface**
  - Two digital PWM outpus (DSPK) with support for two single–ended L/R channels and one differential mono channel
  - One DMIC interface with left and right channel input
  - One I2S interface with input/ output and TDM support
- **General Interface**
  - One USB2.0 port, configurable as DEVICE/ HOST
  - One EMAC interface with support for 100M RMII and IEEE1588 protocol
  - Three QSPI interfaces for standard, dual SPI and quad SPI, configurable as Master/ Slave
  - One SPI for standard SPI interface, configurable as Master/ Slave
  - Eight 2/ 3 / 4–way UART interfaces compatible with industry standard 16550 and up to 5 Mbps of baud rate
  - Three 7–bit and 10–bit I2C interfaces with up to 400 Kb/s of addressing rate
  - Two CAN modules with support for CAN2.0A and CAN2.0, and up to 1 Mbps of programmable comminicatable speed
  - One CIR that supports infrared input and output
  - One PBUS with support of 16–bit 100–MHz clock for read and 100 MB/s of write access to the address space of external devices
  - Five GPIO interfaces with a total of 84 IOs individually configurable
    - Resistor options: no pullup, pullup 33KΩ, pulldown 33KΩ
    - Eight output driver levels available
    - Two–level dithering and interrupts
    - Bit operation
- **Timer**
  - GTC Generic Timers
    - 52–bit timer for system heartbeat clock with over 35 years of clocking cycle
    - Pause or Resume timer configurable in debug mode
  - WDOG
    - Interrupt and reset mode with configurable timeout period from 1ms to 37 hours
    - Pause or Resume timer configurable in debug mode
    - Firmware write protection
  - Real Time Clock (RTC)
    - Unit in seconds and time span of 100 years with support of alarm settings
    - Support for an external 32.768–KHz oscillator for digital calibration within the range of ± 975 ppm
    - Independent standby power supply input pin for built–in power switch
    - 128–bit register reserved for system data backup suck as key protected data during power down
    - Less than 2.3 uA of RTC operating current
  - PWM
    - Built–in 16–bit counter with four timers
    - Support for up to eight independent PWM channels or four complementary PWM channels
  - EPWM

- Built–in 16–bit PWM timer with 12–way timers
- Support for up to 24 independent PWM channels or 12 complementary PWM channels
- Support for ADC samling triggered by firmware
- Support for fixed number of pulses
- EPWM0~5 support 156–ps high–precision PWM

◦ CAP

- Built–in 32–bit CAP counter with six timers
- Up to six–way CAP input capture or six simple PWM outputs
- Continuous capture or single capture mode available

• **Analog**

◦ Built–in 12–channel 12–bit PSADC, with a maximum sampling rate of 2 Msps.

◦ Built–in 8–channel 12–bit GPADC, with a maximum sampling rate of 2 Msps.

◦ Integrated resistive touch pannel (RTP)

• **Clock and Power**

◦ External Clock Source

- Built–in ± 2% OSC24M. Crystal–free design is supported for some packaging models
- External 24–MHz crystal supported

◦ Four built–in PLLs in CMU:

- PLL_INT0 for CPU only
- PLL_INT1 for BUS, internal modules, and low speed interface units
- PLL_FRA0 for memory interfaces with the spread spectrum feature
- PLL_FRA2 for display output modules with the spread spectrum feature

◦ Three built–in LDO modules for SYSCFG:

- LDO25 (2.5 V 100 mA), for power supply of system reset boot, ADC and eFuse
- Built–in LDO18 (1.8 V 100 mA) for power supply of PSRAM IO and PSRAM
- LDO1x (0.9~1.9 V 500 mA, 50 mV for each), for IO power supply of VDD11_SYS modules

◦ Built–in THS for high and low temperature interrupt alarms and over–temperature protection

3. Product Information

Table 3–1 Product

Model	Feature	Package	Temperature
D133BBS	512 KB SRAM 8 MB PSRAM	QFN68, 7 x 7 x 0.85 mm, with an interval of 0.35 mm	–40 to +105℃
D133CBS	1 MB SRAM 8 MB PSRAM	QFN88, 10 x 10 x 0.85 mm, with an interval of 0.4 mm	–40 to +105℃
D133CCS	1 MB SRAM 16 MB PSRAM	QFN88, 10 x 10 x 0.85 mm, with an interval of 0.4 mm	–40 to +105℃
D133EBS	1 MB SRAM 8 MB PSRAM	QFN100, 12 x 12 x 0.85 mm, with an interval of 0.4 mm	–40 to +105℃
D133ECS	1 MB SRAM 16 MB PSRAM	QFN100, 12 x 12 x 0.85 mm, with an interval of 0.4 mm	–40 to +105℃

Table 3–2 Product Comparison

Item	D133BBS	D133CBS D133CCS	D133EBS D133ECS
CPU	E907 480MHz@1.1 V	E907 480MHz@1.1 V	E907 480MHz@1.1 V
Safety	Support	Support	Support
Clock	Built–in OSC	External crystal oscillator	External crystal oscillator
RGB	x 1	x 1	x 1
LVDS	x 1	x 1	x 1
MIPI DSI	x 1	x 1	x 1
RTP	x 1	x 1	x 1
DVP	–	x 1	x 1
RTC	–	x 1	x 1
SD3.01	x 1	x 1	x 1
eMMC 4.41/ SDIO 3.0	x 1	x 1	x 1
DMIC	x 2	x 2	x 2
I2S	x 1	x 1	x 1
DSPK	x 2	x 2	x 2
QSPI	x 3	x 3	x 3
SPI	x 1	x 1	x 1
UART	x 8	x 8	x 8
I2C	x 3	x 3	x 3
CAN	–	x 1	x 2

Table 3–2 Product Comparison (continued)

Item	D133BBS	D133CBS D133CCS	D133EBS D133ECS
CIR	x 1	x 1	x 1
EMAC–100M	–	x 1	x 1
USB2.0	–	x 1	x 1
PWM	x 4 (8 ch)	x 4 (8 ch)	x 4 (8 ch)
EPWM	x 12 (24 ch)	x 12 (24 ch)	x 12 (24 ch)
CAP	x 6	x 6	x 6
ADC	x 2 (10 ch)	x 2 (10 ch)	x 2 (12 ch)

4. Electrical Features

4.1. Operating Conditions

4.1.1. Maximum Values

Table 4–1 Maximum limit for electrical parameters

Symbol	Description	Minimum	Maximum	Unit
Tstg	Storage temperature	–40	125	° C
For VCC33_IO	GPIO Power	–0.3	3.6	V
RTC_VCOIN	RTC power source	–0.3	3.6	V
VDD11_SYS	Kernel and system power supply	–0.3	1.32	V
Iio	IO input/output current	–55	60	mA

4.1.2. Recommended Operating Conditions

Table 4–2 Recommended values

Symbol	Description	Minimum	Typical	Maximum	Unit
Tj	Junction temperature	–40	–	105	° C
Ta	Ambient temperature	–40	–	85	° C
For VCC33_IO	GPIO Power	3.0	3.3	3.6	V
RTC_VCOIN	RTC power source	2.7	3.0	For VCC33_IO	V
VDD11_SYS	Kernel and system power supply	0.99	1.1	1.21	V

4.2. RTC Power Supply

RTC is powered by VCC33_IO1 and VCOIN. In system design, the internal circuit automatically checks and compares the voltages of VCC33_IO and VCOIN, and chooses the circuit with the higher voltage for power supply.

- When power is on, the typical voltage is 3.3 V for VCC33_IO and 3.0 V for VCOIN which is powered by button cells. In this case, the voltage of VCC33_IO is higher than that of VCOIN, and thus RTC is powered by VCC33_IO.
- When power is off, VCC33_IO is not powered, and VCOIN becomes the only power source. The typical voltage powered by button cells is 3.0 V, and thus RTC is powered by VCOIN. In this case, the typical operating current of RTC is 2.3 uA, which helps to prolong the service life of button cells.

For external power supply, VCOIN needs to be connected with an RC delay power–on circuit (10 KΩ / 0.1 uF). This solution can ensure a smooth transition of power supply for RTC during power–on or power–off, and avoid damages to RTC caused by sudden voltage changes.

4.3. Power–on/Power–off Sequence and Reset

4.3.1. Power–on/Power–off Sequence

There is no power–on and power–off sequence requirement for VCC33_IO, VDD11_SYS and LDO18. The rising edge working at VCC33_IO shall be detected after 150 us.

4.3.2. Reset Source

When any of the following reset conditions is met, the chip will reset:

- SYS power-on reset: a reset is triggered when VCC33_IO and VDD11_SYS are powered on. The system automatically releases the reset within 10 ms after power on.
- RTC power-on reset: a reset is automatically completed when RTC powers on (by VCC33_IO and VCOIN).
- External pin reset: a reset is triggered when the RESETN pin is driven low for over 2 ms.
- Debugger reset: a reset is immediately triggered upon receiving the RESET signal from JTAG IO.
- Watchdog reset: when the reset is enabled, a reset is immediately triggered when the configured timeout reset conditions are met in WDOG.
- Over-temperature reset: when the reset is enabled by software, a reset is immediately triggered when the temperature is higher than the configured temperature in THS.
- Voltage comparison reset: when the reset is enabled, a reset is immediately triggered when the voltage of RTC_IO is either higher or lower (configurable) than the referenced voltage.

4.4. Built-in LDO Electrical Features

4.4.1. LDO25

The built-in LDO25 is a configable linear regulator used for stable power supply of system analog, GPADC, PSADC eFuse. Its electrical characteristics are as follows: In addition, LDO25 is also used as the referenced voltage for GPADC/ PSADC and Its electrical characteristics are as follows:

Table 4-3 LDO25 Electrical Features

Symbol	Description	Minimum	Typical	Maximum	Unit
Vo	Output voltage	2.4	2.5	3.1	V
Io	Output current	–	–	100	mA
Co	External decoupling capacitor	–	1	–	uF

4.4.2. LDO18

The built-in LDO18 is a configurable low-voltage linear regulator used for stable power supply of PSRAM IO/ PSRAM. Its electrical characteristics are as follows:

Table 4-4 LDO18 Electrical Features

Symbol	Description	Minimum	Typical	Maximum	Unit
Vo	Output voltage	1.71	1.8	1.92	V
Io	Output current	–	–	100	mA
Co	External decoupling capacitor	–	1	–	uF

4.4.3. LDO1x

The built–in LDO1x is a configurable low–voltage linear regulator used for stable power supply of VDD11_SYS. Its electrical characteristics are as follows:

Table 4–5 LDO1x Electrical Features

Symbol	Description	Minimum	Typical	Maximum	Unit
Vo	Output voltage	0.9	1.1	1.9	V
Io	Output current	–	–	500	mA
Co	External decoupling capacitor	–	1	–	uF

4.5. Clock

External Clock Source

- 32.768 KHz clock: for low frequency and RTC.
- 24.000 KHz clock: for low frequency and RTC.

Symbol	Description	Minimum	Typical	Maximum	Unit
OSC_24M	PLL clock source	–	24	–	MHz
OSC_32K	RTC clock source	–	32768	–	Hz

4.6. IO Electrical Features

Table 4–6 GPIO DC Electrical Features

Symbol	Description	Minimum	Typical	Maximum	Unit
VIH	High–level input voltage	0.7 * VCC33_IO	–	VCC33_IO + 0.3	V
VIL	Low–level input voltage	– 0.3	–	0.3 * VCC33_IO	V
RPU	Pullup resistor	–	33	–	KΩ
RPD	Pulldown resistor	–	33	–	KΩ
IIH	High–level input current	–	–	10	uA
IIL	Low–level input current	–	–	10	uA
VOH	High–level output voltage	VCC33_IO + 0.3	–	For VCC33_IO	V
VOL	Low–level output voltage	0	–	0.3	V
IOH	High–level output current	8	–	60	mA
IOL	Low–level output current	8	–	55	mA
IOZ	Tri–stated output leakage current	–10	–	10	uA
CIN	Input capacitance	–	–	5	pF
COUT	Output capacitance	–	–	5	pF

Table 4–7 GPIO AC Electrical Features

Symbol	Description	Test Conditions	Minimum	Typical	Maximum	Unit
fmax	Maximum frequency	6pF of load capacitance	–	–	150	MHz
TR230	Rise time	Time between VOL and VOH	–	–	1.6	ns

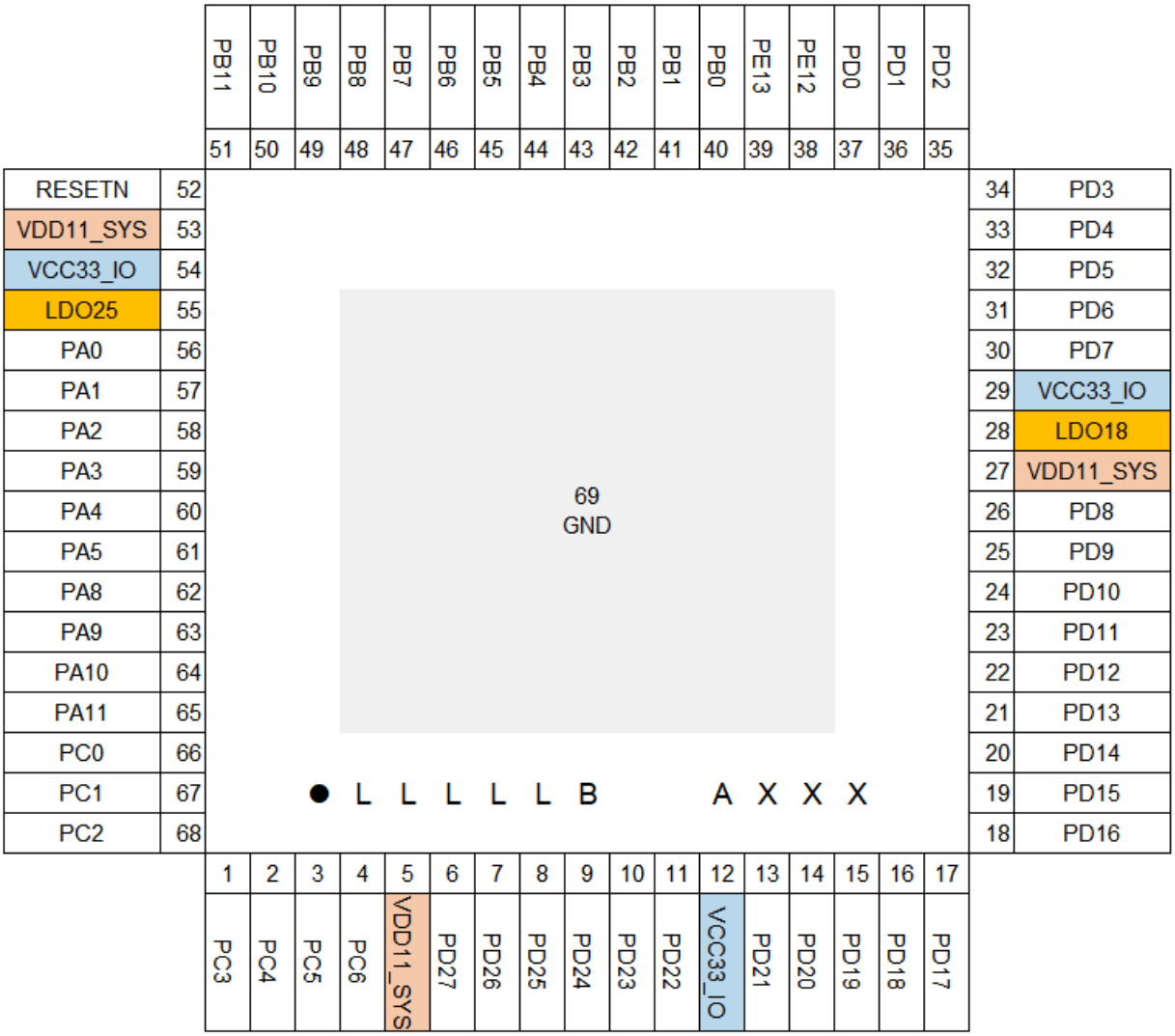
Table 4–7 GPIO AC Electrical Features (continued)

Symbol	Description	Test Conditions	Minimum	Typical	Maximum	Unit
tf	Fall time	Time between VOH and VOL	–	–	1.6	ns

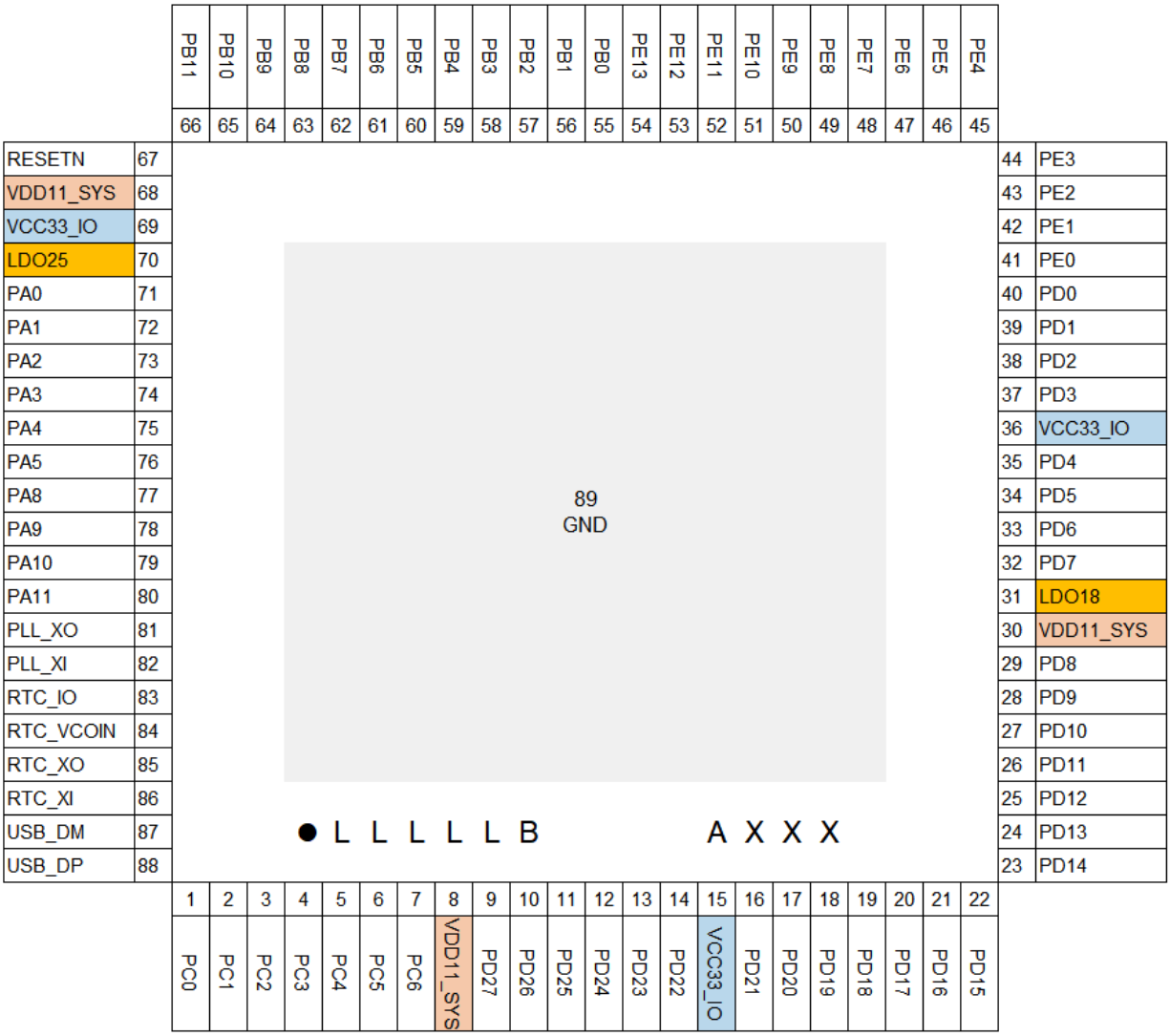
5. Package Information

5.1. Pin Distribution

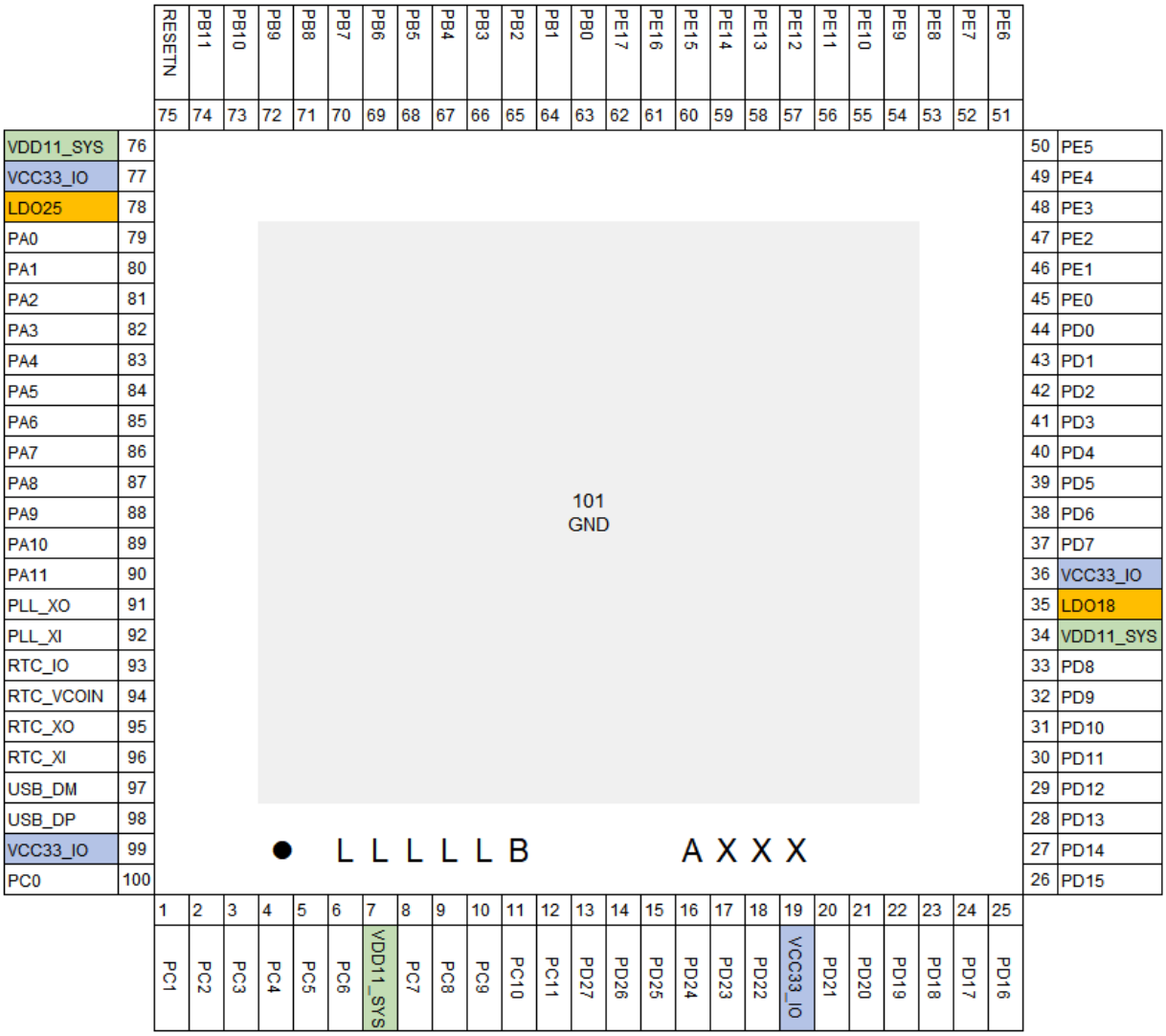
5.1.1. D133BxS QFN68



5.1.2. D133CxS QFN88



5.1.3. D133ExS QFN100



LLLLLB: LLLLL indicates bacth number, and B is a fixed letter.

AXXX: XXX indictaes date code, and A is a fixed letter.

5.2. Pin Attributes

Note:

- [1]: Serial number of pin in the package
- [2]: Name of pin in the package
- [3]: Signal Type, to indicate signal directions
  - I – Input
  - O – Output
  - I/O – Input/ Output
  - A – Analog
  - AI – Analog Input
  - AO – Analog Output

◦ P – Power

◦ G – Ground

• [4]: Pin reset status, PU means pullup, PD means pulldown, and Z means high impedance state.

• [5]: PU/PD means there are internal pullup and pulldown resistors which can be enable and disable by software.

• [6]: Default output current. For GPIO, the default output current is 20 mA and the maximum is 50 mA.

• [7]: Power source

5.2.1. D133BxS QFN68

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source[7]
GPIO A						
56	PA0	I/O	Z	PU/PD	20	For VCC33_IO
57	PA1	I/O	Z	PU/PD	20	For VCC33_IO
58	PA2	I/O	Z	PU/PD	20	For VCC33_IO
59	PA3	I/O	Z	PU/PD	20	For VCC33_IO
60	PA4	I/O	Z	PU/PD	20	For VCC33_IO
61	PA5	I/O	Z	PU/PD	20	For VCC33_IO
62	PA8	I/O	PU	PU/PD	20	For VCC33_IO
63	PA9	I/O	PU	PU/PD	20	For VCC33_IO
64	PA10	I/O	PU	PU/PD	20	For VCC33_IO
65	PA11	I/O	PU	PU/PD	20	For VCC33_IO
GPIO B						
40	PB0	I/O	Z	PU/PD	20	For VCC33_IO
41	PB1	I/O	Z	PU/PD	20	For VCC33_IO
42	PB2	I/O	Z	PU/PD	20	For VCC33_IO
43	PB3	I/O	Z	PU/PD	20	For VCC33_IO
44	PB4	I/O	Z	PU/PD	20	For VCC33_IO
45	PB5	I/O	Z	PU/PD	20	For VCC33_IO
46	PB6	I/O	Z	PU/PD	20	For VCC33_IO
47	PB7	I/O	Z	PU/PD	20	For VCC33_IO
48	PB8	I/O	Z	PU/PD	20	For VCC33_IO
49	PB9	I/O	Z	PU/PD	20	For VCC33_IO
50	PB10	I/O	Z	PU/PD	20	For VCC33_IO
51	PB11	I/O	Z	PU/PD	20	For VCC33_IO
GPIO C						
66	PC0	I/O	Z	PU/PD	20	For VCC33_IO
67	PC1	I/O	Z	PU/PD	20	For VCC33_IO
68	PC2	I/O	Z	PU/PD	20	For VCC33_IO
1	PC3	I/O	Z	PU/PD	20	For VCC33_IO
2	PC4	I/O	Z	PU/PD	20	For VCC33_IO

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source[7]
3	PC5	I/O	Z	PU/PD	20	For VCC33_IO
4	PC6	I/O	Z	PU/PD	20	For VCC33_IO
GPIO D						
37	PD0	I/O	Z	PU/PD	20	For VCC33_IO
36	PD1	I/O	Z	PU/PD	20	For VCC33_IO
35	PD2	I/O	Z	PU/PD	20	For VCC33_IO
34	PD3	I/O	Z	PU/PD	20	For VCC33_IO
33	PD4	I/O	Z	PU/PD	20	For VCC33_IO
32	PD5	I/O	Z	PU/PD	20	For VCC33_IO
31	PD6	I/O	Z	PU/PD	20	For VCC33_IO
30	PD7	I/O	Z	PU/PD	20	For VCC33_IO
26	PD8	I/O	Z	PU/PD	20	For VCC33_IO
25	PD9	I/O	Z	PU/PD	20	For VCC33_IO
24	PD10	I/O	Z	PU/PD	20	For VCC33_IO
23	PD11	I/O	Z	PU/PD	20	For VCC33_IO
22	PD12	I/O	Z	PU/PD	20	For VCC33_IO
21	PD13	I/O	Z	PU/PD	20	For VCC33_IO
20	PD14	I/O	Z	PU/PD	20	For VCC33_IO
19	PD15	I/O	Z	PU/PD	20	For VCC33_IO
18	PD16	I/O	Z	PU/PD	20	For VCC33_IO
17	PD17	I/O	Z	PU/PD	20	For VCC33_IO
16	PD18	I/O	Z	PU/PD	20	For VCC33_IO
15	PD19	I/O	Z	PU/PD	20	For VCC33_IO
14	PD20	I/O	Z	PU/PD	20	For VCC33_IO
13	PD21	I/O	Z	PU/PD	20	For VCC33_IO
11	PD22	I/O	Z	PU/PD	20	For VCC33_IO
10	PD23	I/O	Z	PU/PD	20	For VCC33_IO
9	PD24	I/O	Z	PU/PD	20	For VCC33_IO
8	PD25	I/O	Z	PU/PD	20	For VCC33_IO
7	PD26	I/O	Z	PU/PD	20	For VCC33_IO
6	PD27	I/O	Z	PU/PD	20	For VCC33_IO
GPIO E						
38	PE12	I/O	Z	PU/PD	20	For VCC33_IO
39	PE13	I/O	Z	PU/PD	20	For VCC33_IO
PLL						
52	RESETN	I	–	–	–	–
Power						
12, 29, 54	For VCC33_IO	P	–	–	–	–
55	LDO25	P	–	–	–	–
28	LDO18	P	–	–	–	–
5, 27, 53	VDD11_SYS	P	–	–	–	–

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source[7]
69	GND	P	–	–	–	–

5.2.2. D133CxS QFN88

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source[7]
GPIO A						
71	PA0	I/O	Z	PU/PD	20	For VCC33_IO
72	PA1	I/O	Z	PU/PD	20	For VCC33_IO
73	PA2	I/O	Z	PU/PD	20	For VCC33_IO
74	PA3	I/O	Z	PU/PD	20	For VCC33_IO
75	PA4	I/O	Z	PU/PD	20	For VCC33_IO
76	PA5	I/O	Z	PU/PD	20	For VCC33_IO
77	PA8	I/O	PU	PU/PD	20	For VCC33_IO
78	PA9	I/O	PU	PU/PD	20	For VCC33_IO
79	PA10	I/O	PU	PU/PD	20	For VCC33_IO
80	PA11	I/O	PU	PU/PD	20	For VCC33_IO
GPIO B						
55	PB0	I/O	Z	PU/PD	20	For VCC33_IO
56	PB1	I/O	Z	PU/PD	20	For VCC33_IO
57	PB2	I/O	Z	PU/PD	20	For VCC33_IO
58	PB3	I/O	Z	PU/PD	20	For VCC33_IO
59	PB4	I/O	Z	PU/PD	20	For VCC33_IO
60	PB5	I/O	Z	PU/PD	20	For VCC33_IO
61	PB6	I/O	Z	PU/PD	20	For VCC33_IO
62	PB7	I/O	Z	PU/PD	20	For VCC33_IO
63	PB8	I/O	Z	PU/PD	20	For VCC33_IO
64	PB9	I/O	Z	PU/PD	20	For VCC33_IO
65	PB10	I/O	Z	PU/PD	20	For VCC33_IO
66	PB11	I/O	Z	PU/PD	20	For VCC33_IO
GPIO C						
1	PC0	I/O	Z	PU/PD	20	For VCC33_IO
2	PC1	I/O	Z	PU/PD	20	For VCC33_IO
3	PC2	I/O	Z	PU/PD	20	For VCC33_IO
4	PC3	I/O	Z	PU/PD	20	For VCC33_IO
5	PC4	I/O	Z	PU/PD	20	For VCC33_IO
6	PC5	I/O	Z	PU/PD	20	For VCC33_IO
7	PC6	I/O	Z	PU/PD	20	For VCC33_IO
GPIO D						
40	PD0	I/O	Z	PU/PD	20	For VCC33_IO
39	PD1	I/O	Z	PU/PD	20	For VCC33_IO
38	PD2	I/O	Z	PU/PD	20	For VCC33_IO

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source[7]
37	PD3	I/O	Z	PU/PD	20	For VCC33_IO
35	PD4	I/O	Z	PU/PD	20	For VCC33_IO
34	PD5	I/O	Z	PU/PD	20	For VCC33_IO
33	PD6	I/O	Z	PU/PD	20	For VCC33_IO
32	PD7	I/O	Z	PU/PD	20	For VCC33_IO
29	PD8	I/O	Z	PU/PD	20	For VCC33_IO
28	PD9	I/O	Z	PU/PD	20	For VCC33_IO
27	PD10	I/O	Z	PU/PD	20	For VCC33_IO
26	PD11	I/O	Z	PU/PD	20	For VCC33_IO
25	PD12	I/O	Z	PU/PD	20	For VCC33_IO
24	PD13	I/O	Z	PU/PD	20	For VCC33_IO
23	PD14	I/O	Z	PU/PD	20	For VCC33_IO
22	PD15	I/O	Z	PU/PD	20	For VCC33_IO
21	PD16	I/O	Z	PU/PD	20	For VCC33_IO
20	PD17	I/O	Z	PU/PD	20	For VCC33_IO
19	PD18	I/O	Z	PU/PD	20	For VCC33_IO
18	PD19	I/O	Z	PU/PD	20	For VCC33_IO
17	PD20	I/O	Z	PU/PD	20	For VCC33_IO
16	PD21	I/O	Z	PU/PD	20	For VCC33_IO
14	PD22	I/O	Z	PU/PD	20	For VCC33_IO
13	PD23	I/O	Z	PU/PD	20	For VCC33_IO
12	PD24	I/O	Z	PU/PD	20	For VCC33_IO
11	PD25	I/O	Z	PU/PD	20	For VCC33_IO
10	PD26	I/O	Z	PU/PD	20	For VCC33_IO
9	PD27	I/O	Z	PU/PD	20	For VCC33_IO
GPIO E						
41	PE0	I/O	Z	PU/PD	20	For VCC33_IO
42	PE1	I/O	Z	PU/PD	20	For VCC33_IO
43	PE2	I/O	Z	PU/PD	20	For VCC33_IO
44	PE3	I/O	Z	PU/PD	20	For VCC33_IO
45	PE4	I/O	Z	PU/PD	20	For VCC33_IO
46	PE5	I/O	Z	PU/PD	20	For VCC33_IO
47	PE6	I/O	Z	PU/PD	20	For VCC33_IO
48	PE7	I/O	Z	PU/PD	20	For VCC33_IO
49	PE8	I/O	Z	PU/PD	20	For VCC33_IO
50	PE9	I/O	Z	PU/PD	20	For VCC33_IO
51	PE10	I/O	Z	PU/PD	20	For VCC33_IO
52	PE11	I/O	Z	PU/PD	20	For VCC33_IO
53	PE12	I/O	Z	PU/PD	20	For VCC33_IO
54	PE13	I/O	Z	PU/PD	20	For VCC33_IO
RTC						

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source[7]
83	RTC_IO	OD	–	–	–	–
84	RTC_VCOIN	P	–	–	–	–
85	RTC_XO	O	–	–	–	–
86	RTC_XI	I	–	–	–	–
PLL						
67	RESETN	I	–	–	–	–
81	PLL_XO	O	–	–	–	–
82	PLL_XI	I	–	–	–	–
USB						
87	USB_DM	A	–	–	–	–
88	USB_DP	A	–	–	–	–
Power						
15, 36, 69	For VCC33_IO	P	–	–	–	–
70	LDO25	P	–	–	–	–
31	LDO18	P	–	–	–	–
8, 30, 68	VDD11_SYS	P	–	–	–	–
89	GND	P	–	–	–	–

5.2.3. D133ExS QFN100

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
GPIO A						
79	PA0	I/O	Z	PU/PD	20	For VCC33_IO
80	PA1	I/O	Z	PU/PD	20	For VCC33_IO
81	PA2	I/O	Z	PU/PD	20	For VCC33_IO
82	PA3	I/O	Z	PU/PD	20	For VCC33_IO
83	PA4	I/O	Z	PU/PD	20	For VCC33_IO
84	PA5	I/O	Z	PU/PD	20	For VCC33_IO
85	PA6	I/O	Z	PU/PD	20	For VCC33_IO
86	PA7	I/O	Z	PU/PD	20	For VCC33_IO
87	PA8	I/O	PU	PU/PD	20	For VCC33_IO
88	PA9	I/O	PU	PU/PD	20	For VCC33_IO
89	PA10	I/O	PU	PU/PD	20	For VCC33_IO
90	PA11	I/O	PU	PU/PD	20	For VCC33_IO
GPIO B						
63	PB0	I/O	Z	PU/PD	20	For VCC33_IO
64	PB1	I/O	Z	PU/PD	20	For VCC33_IO
65	PB2	I/O	Z	PU/PD	20	For VCC33_IO
66	PB3	I/O	Z	PU/PD	20	For VCC33_IO
67	PB4	I/O	Z	PU/PD	20	For VCC33_IO
68	PB5	I/O	Z	PU/PD	20	For VCC33_IO

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
69	PB6	I/O	Z	PU/PD	20	For VCC33_IO
70	PB7	I/O	Z	PU/PD	20	For VCC33_IO
71	PB8	I/O	Z	PU/PD	20	For VCC33_IO
72	PB9	I/O	Z	PU/PD	20	For VCC33_IO
73	PB10	I/O	Z	PU/PD	20	For VCC33_IO
74	PB11	I/O	Z	PU/PD	20	For VCC33_IO
GPIO C						
100	PC0	I/O	Z	PU/PD	20	For VCC33_IO
1	PC1	I/O	Z	PU/PD	20	For VCC33_IO
2	PC2	I/O	Z	PU/PD	20	For VCC33_IO
3	PC3	I/O	Z	PU/PD	20	For VCC33_IO
4	PC4	I/O	Z	PU/PD	20	For VCC33_IO
5	PC5	I/O	Z	PU/PD	20	For VCC33_IO
6	PC6	I/O	Z	PU/PD	20	For VCC33_IO
8	PC7	I/O	Z	PU/PD	20	For VCC33_IO
9	PC8	I/O	Z	PU/PD	20	For VCC33_IO
10	PC9	I/O	Z	PU/PD	20	For VCC33_IO
11	PC10	I/O	Z	PU/PD	20	For VCC33_IO
12	PC11	I/O	Z	PU/PD	20	For VCC33_IO
GPIO D						
44	PD0	I/O	Z	PU/PD	20	For VCC33_IO
43	PD1	I/O	Z	PU/PD	20	For VCC33_IO
42	PD2	I/O	Z	PU/PD	20	For VCC33_IO
41	PD3	I/O	Z	PU/PD	20	For VCC33_IO
40	PD4	I/O	Z	PU/PD	20	For VCC33_IO
39	PD5	I/O	Z	PU/PD	20	For VCC33_IO
38	PD6	I/O	Z	PU/PD	20	For VCC33_IO
37	PD7	I/O	Z	PU/PD	20	For VCC33_IO
33	PD8	I/O	Z	PU/PD	20	For VCC33_IO
32	PD9	I/O	Z	PU/PD	20	For VCC33_IO
31	PD10	I/O	Z	PU/PD	20	For VCC33_IO
30	PD11	I/O	Z	PU/PD	20	For VCC33_IO
29	PD12	I/O	Z	PU/PD	20	For VCC33_IO
28	PD13	I/O	Z	PU/PD	20	For VCC33_IO
27	PD14	I/O	Z	PU/PD	20	For VCC33_IO
26	PD15	I/O	Z	PU/PD	20	For VCC33_IO
25	PD16	I/O	Z	PU/PD	20	For VCC33_IO
24	PD17	I/O	Z	PU/PD	20	For VCC33_IO
23	PD18	I/O	Z	PU/PD	20	For VCC33_IO
22	PD19	I/O	Z	PU/PD	20	For VCC33_IO
21	PD20	I/O	Z	PU/PD	20	For VCC33_IO

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
20	PD21	I/O	Z	PU/PD	20	For VCC33_IO
18	PD22	I/O	Z	PU/PD	20	For VCC33_IO
17	PD23	I/O	Z	PU/PD	20	For VCC33_IO
16	PD24	I/O	Z	PU/PD	20	For VCC33_IO
15	PD25	I/O	Z	PU/PD	20	For VCC33_IO
14	PD26	I/O	Z	PU/PD	20	For VCC33_IO
13	PD27	I/O	Z	PU/PD	20	For VCC33_IO
GPIO E						
45	PE0	I/O	Z	PU/PD	20	For VCC33_IO
46	PE1	I/O	Z	PU/PD	20	For VCC33_IO
47	PE2	I/O	Z	PU/PD	20	For VCC33_IO
48	PE3	I/O	Z	PU/PD	20	For VCC33_IO
49	PE4	I/O	Z	PU/PD	20	For VCC33_IO
50	PE5	I/O	Z	PU/PD	20	For VCC33_IO
51	PE6	I/O	Z	PU/PD	20	For VCC33_IO
52	PE7	I/O	Z	PU/PD	20	For VCC33_IO
53	PE8	I/O	Z	PU/PD	20	For VCC33_IO
54	PE9	I/O	Z	PU/PD	20	For VCC33_IO
55	PE10	I/O	Z	PU/PD	20	For VCC33_IO
56	PE11	I/O	Z	PU/PD	20	For VCC33_IO
57	PE12	I/O	Z	PU/PD	20	For VCC33_IO
58	PE13	I/O	Z	PU/PD	20	For VCC33_IO
59	PE14	I/O	Z	PU/PD	20	For VCC33_IO
60	PE15	I/O	Z	PU/PD	20	For VCC33_IO
61	PE16	I/O	Z	PU/PD	20	For VCC33_IO
62	PE17	I/O	Z	PU/PD	20	For VCC33_IO
RTC						
93	RTC_IO	OD	–	–	–	–
94	RTC_VCOIN	P	–	–	–	–
95	RTC_XO	O	–	–	–	–
96	RTC_XI	I	–	–	–	–
PLL						
75	RESETN	I	–	–	–	–
91	PLL_XO	O	–	–	–	–
92	PLL_XI	I	–	–	–	–
USB						
97	USB_DM	A	–	–	–	–
98	USB_DP	A	–	–	–	–
Power						
19, 36, 77, 99	For VCC33_IO	P	–	–	–	–
78	LDO25	P	–	–	–	–

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA) [6]	Power Source [7]
35	LDO18	P	–	–	–	–
7, 34, 76	VDD11_SYS	P	–	–	–	–
101	GND	P	–	–	–	–

5.3. Pin–Mux

Table 5–1 D13x Pin–mux

Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX	–	PSADC0	CPU_NMI
PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX	–	PSADC1	DE_TE
PA2	GPADC2	–	I2C1_SCL	UART1_TX	–	PSADC2	UART2_CTS
PA3	GPADC3	–	I2C1_SDA	UART1_RX	–	PSADC3	UART2_RTS
PA4	GPADC4	–	CAN0_TX	UART2_TX	–	PSADC4	–
PA5	GPADC5	–	CAN0_RX	UART2_RX	–	PSADC5	RTC_32K
PA6	GPADC6	–	CAN1_TX	UART3_TX	–	PSADC6	–
PA7	GPADC7	–	CAN1_RX	UART3_RX	–	PSADC7	–
PA8	RTP_XP	–	I2C2_SCL	–	–	PSADC8	–
PA9	RTP_YP	–	I2C2_SDA	–	–	PSADC9	–
PA10	RTP_XN	IR_RX	–	–	–	PSADC10	JTAG_MS
PA11	RTP_YN	IR_TX	–	–	–	PSADC11	JTAG_CK
PB0	SPI0_WP	SPI1_WP	–	UART4_TX	–	–	–
PB1	SPI0_MISO	SPI1_MISO	–	UART6_TX	–	–	–
PB2	SPI0_CS0	SPI1_CS0	–	UART6_RX	–	–	–
PB3	SPI0_HOLD	SPI1_HOLD	–	UART4_RX	–	–	–
PB4	SPI0_CLK	SPI1_CLK	–	UART6_RTS	–	–	–
PB5	SPI0_MOSI	SPI1_MOSI	–	UART4_RTS	UART6_CTS	–	–
PB6	SDC0_CMD	SPI2_CS	–	UART5_TX	–	–	FLASH_CS
PB7	SDC0_CLK	SPI2_MISO	–	UART5_RX	–	–	FLASH_MISO
PB8	SDC0_D3	SPI2_MOSI	–	UART5_RTS	UART7_CTS	–	FLASH_MOSI
PB9	SDC0_D0	SPI2_CLK	–	UART7_RTS	–	–	FLASH_CLK
PB10	SDC0_D1	SPI2_HOLD	–	UART7_TX	–	–	–
PB11	SDC0_D2	SPI2_WP	SPI0_CS1	UART7_RX	–	–	–
PC0	SDC1_D1	–	I2C2_SCL	UART3_RTS	–	–	JTAG_MS
PC1	SDC1_D0	–	–	–	–	–	–
PC2	SDC1_CLK	–	–	–	–	–	UART0_TX
PC3	SDC1_CMD	–	–	–	–	–	–
PC4	SDC1_D3	–	I2C1_SCL	UART3_TX	–	–	UART0_RX
PC5	SDC1_D2	–	I2C1_SDA	UART3_RX	–	–	JTAG_CK
PC6	SDC1_DET	CAP0	I2C2_SDA	UART3_CTS	DE_TE	CLK_OUT3	–
PC7	–	CAP1	–	–	–	–	–
PC8	SPI3_CLK	CAP2	CAN0_TX	UART4_TX	–	–	–
PC9	SPI3_CS0	CAP3	CAN0_RX	UART4_RX	–	–	–

Table 5–1 D13x Pin–mux (continued)

Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
PC10	SPI3_MOSI	CAP4	CAN1_TX	UART5_TX	–	–	–
PC11	SPI3_MISO	CAP5	CAN1_RX	UART5_RX	–	–	–
PD0	LCD_D0	SPI3_CLK	I2C0_SCL	UART0_TX	PBUS_AD0	EPWM11_B	–
PD1	LCD_D1	SPI3_CS0	I2C0_SDA	UART0_RX	PBUS_AD1	EPWM11_A	–
PD2	LCD_D2	SPI3_MOSI	I2C1_SCL	UART1_TX	PBUS_AD2	EPWM10_B	–
PD3	LCD_D3	SPI3_MISO	I2C1_SDA	UART1_RX	PBUS_AD3	EPWM10_A	–
PD4	LCD_D4	SPI1_CS0	I2C2_SCL	UART2_TX	PBUS_AD4	–	–
PD5	LCD_D5	SPI1_MISO	I2C2_SDA	UART2_RX	PBUS_AD5	–	–
PD6	LCD_D6	SPI1_MOSI	PWM0_A	DSPK0	PBUS_AD6	–	–
PD7	LCD_D7	SPI1_CLK	PWM0_B	DSPK1	PBUS_AD7	–	–
PD8	LCD_D8	SPI1_HOLD	PWM1_A	–	PBUS_CLK	EPWM9_B	–
PD9	LCD_D9	SPI1_WP	–	–	PBUS_NCS	EPWM9_A	–
PD10	LCD_D10	CAP5	–	–	PBUS_NADV	EPWM8_B	–
PD11	LCD_D11	CAP4	I2S_DIN	–	PBUS_NWE	EPWM8_A	–
PD12	LCD_D12	CAP3	I2S_DOUT	–	PBUS_NOE	EPWM7_B	–
PD13	LCD_D13	CAP2	I2S_LRCK	–	CLK_OUT0	EPWM7_A	–
PD14	LCD_D14	CAP1	I2S_BCLK	–	PBUS_AD8	EPWM6_B	–
PD15	LCD_D15	CAP0	I2S_MCLK	–	PBUS_AD9	EPWM6_A	–
PD16	LCD_D16	PWM1_B	DMIC_CLK	UART2_TX	PBUS_AD10	EPWM5_B	–
PD17	LCD_D17	PWM2_A	DMIC_D0	UART2_RX	PBUS_AD11	EPWM5_A	–
PD18	LCD_D18	LVDS_D0N	DSI_D0N	–	PBUS_AD12	EPWM4_B	–
PD19	LCD_D19	LVDS_D0P	DSI_D0P	–	PBUS_AD13	EPWM4_A	–
PD20	LCD_D20	LVDS_D1N	DSI_D1N	–	PBUS_AD14	EPWM3_B	–
PD21	LCD_D21	LVDS_D1P	DSI_D1P	–	PBUS_AD15	EPWM3_A	–
PD22	LCD_D22	LVDS_D2N	DSI_CKN	–	–	EPWM2_B	–
PD23	LCD_D23	LVDS_D2P	DSI_CKP	–	–	EPWM2_A	–
PD24	LCD_DCLK	LVDS_CKN	DSI_D2N	–	–	EPWM1_B	–
PD25	LCD_HS	LVDS_CKP	DSI_D2P	–	PWM2_B	EPWM1_A	–
PD26	LCD_VS	LVDS_D3N	DSI_D3N	–	PWM3_A	EPWM0_B	–
PD27	LCD_DE	LVDS_D3P	DSI_D3P	–	PWM3_B	EPWM0_A	CMU_CKT
PE0	EMAC_RXD1	DVP_D0	PWM0_A	UART3_TX	–	–	–
PE1	EMAC_RXD0	DVP_D1	PWM0_B	UART3_RX	–	–	–
PE2	EMAC_CRS_DV	DVP_D2	–	UART4_TX	–	–	–
PE3	EMAC_REFCLK	DVP_D3	I2S_MCLK	UART4_RX	–	–	–
PE4	EMAC_TXD1	DVP_D4	–	UART5_TX	–	–	–
PE5	EMAC_TXD0	DVP_D5	–	UART5_RX	–	–	–
PE6	EMAC_TXC	DVP_D6	–	UART6_TX	–	–	–
PE7	EMAC_TXEN	DVP_D7	–	UART6_RX	–	–	–
PE8	EMAC_MDC	DVP_CK	–	UART7_TX	–	–	–
PE9	EMAC_MDIO	DVP_HS	–	UART7_RX	–	–	–
PE10	CLK_OUT2	DVP_VS	I2S_DIN	DMIC_CLK	–	–	–

Table 5–1 D13x Pin–mux (continued)

Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
PE11	CLK_OUT1	PWM1_A	I2S_LRCK	DMIC_D0	–	–	–
PE12	SPI2_CLK	PWM1_B	I2S_BCLK	DSPK1	–	–	–
PE13	SPI2_CS	PWM2_A	I2S_DOUT	DSPK0	–	–	–
PE14	SPI2_MOSI	I2S_MCLK	I2C0_SCK	UART6_TX	–	–	–
PE15	SPI2_MISO	PWM2_B	I2C0_SDA	UART6_RX	–	–	–
PE16	SPI2_HOLD	PWM3_A	–	UART7_TX	–	–	–
PE17	SPI2_WP	PWM3_B	–	UART7_RX	–	–	–
PU0	USB_DM	–	UART0_RX	UART1_RX	–	–	–
PU1	USB_DP	–	UART0_TX	UART1_TX	–	–	–

5.3.1. D133BxS QFN68 Package Pin Description

Table 5–2 D133BxS QFN68 Package Pin Description

Pins	Definition	Signal Type	Function	Remark
SYSTEM				
52	RESETN	INPUT	System Reset	Built in with a 30kΩ pullup resistor and dithering filter which can be floating if not used. If an external capacitor is connected, the recommended load capacitance is less than 4.7 uF.
POWER				
12, 29, 54	For VCC33_IO	POWER	IO Voltage	3.3 –V power supply
55	LDO25	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
28	LDO18	POWER	Built–in LDO output	Used for internal PSRAM modules. If used otherwise, chip cooling must be considered. Connect with a 1–uF bypass capacitor
5, 27, 53	VDD11_SYS	POWER	Chip Core Voltage	1.1 V power supply. If the built–in LDO1x is used, chip cooling must be considered. Pin 53 is LDO1x output.
69	GND	POWER	–	GND Copper full–cover connection via stitching for cooling.

Table 5–3 D133BxS QFN68 Package Pin–mux

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
GPIO A								
56	PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX	–	PSADC0	CPU_NMI
57	PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX	–	PSADC1	DE_TE
58	PA2	GPADC2	–	I2C1_SCL	UART1_TX	–	PSADC2	UART2_CTS
59	PA3	GPADC3	–	I2C1_SDA	UART1_RX	–	PSADC3	UART2_RTS
60	PA4	GPADC4	–		UART2_TX	–	PSADC4	–
61	PA5	GPADC5	–		UART2_RX	–	PSADC5	RTC_32K
62	PA8	RTP_XP	–	I2C2_SCL	–	–	PSADC8	–
63	PA9	RTP_YP	–	I2C2_SDA	–	–	PSADC9	–
64	PA10	RTP_XN	IR_RX	–	–	–	PSADC10	JTAG_MS
65	PA11	RTP_YN	IR_TX	–	–	–	PSADC11	JTAG_CK
GPIO B								
40	PB0	SPI0_WP	SPI1_WP	–	UART4_TX	–	–	–

Table 5–3 D133BxS QFN68 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
41	PB1	SPI0_MISO	SPI1_MISO	–	UART6_TX	–	–	–
42	PB2	SPI0_CS0	SPI1_CS0	–	UART6_RX	–	–	–
43	PB3	SPI0_HOLD	SPI1_HOLD	–	UART4_RX	–	–	–
44	PB4	SPI0_CLK	SPI1_CLK	–	UART6_RTS	–	–	–
45	PB5	SPI0_MOSI	SPI1_MOSI	–	UART4_RTS	UART6_CTS	–	–
46	PB6	SDC0_CMD	SPI2_CS	–	UART5_TX	–	–	–
47	PB7	SDC0_CLK	SPI2_MISO	–	UART5_RX	–	–	–
48	PB8	SDC0_D3	SPI2_MOSI	–	UART5_RTS	UART7_CTS	–	–
49	PB9	SDC0_D0	SPI2_CLK	–	UART7_RTS	–	–	–
50	PB10	SDC0_D1	SPI2_HOLD	–	UART7_TX	–	–	–
51	PB11	SDC0_D2	SPI2_WP	SPI0_CS1	UART7_RX	–	–	–
GPIO C								
66	PC0	SDC1_D1	–	I2C2_SCL	UART3_RTS	–	–	JTAG_MS
67	PC1	SDC1_D0	–	–	–	–	–	–
68	PC2	SDC1_CLK	–	–	–	–	–	UART0_TX
1	PC3	SDC1_CMD	–	–	–	–	–	–
2	PC4	SDC1_D3	–	I2C1_SCL	UART3_TX	–	–	UART0_RX
3	PC5	SDC1_D2	–	I2C1_SDA	UART3_RX	–	–	JTAG_CK
4	PC6	SDC1_DET	CAP0	I2C2_SDA	UART3_CTS	DE_TE	CLK_OUT3	–
GPIO D								
37	PD0	LCD_D0	SPI3_CLK	I2C0_SCL	UART0_TX	PBUS_AD0	EPWM11_B	–
36	PD1	LCD_D1	SPI3_CS0	I2C0_SDA	UART0_RX	PBUS_AD1	EPWM11_A	–
35	PD2	LCD_D2	SPI3_MOSI	I2C1_SCL	UART1_TX	PBUS_AD2	EPWM10_B	–
34	PD3	LCD_D3	SPI3_MISO	I2C1_SDA	UART1_RX	PBUS_AD3	EPWM10_A	–
33	PD4	LCD_D4	SPI1_CS0	I2C2_SCL	UART2_TX	PBUS_AD4	–	–
32	PD5	LCD_D5	SPI1_MISO	I2C2_SDA	UART2_RX	PBUS_AD5	–	–
31	PD6	LCD_D6	SPI1_MOSI	PWM0_A	DSPK0	PBUS_AD6	–	–
30	PD7	LCD_D7	SPI1_CLK	PWM0_B	DSPK1	PBUS_AD7	–	–
26	PD8	LCD_D8	SPI1_HOLD	PWM1_A	–	PBUS_CLK	EPWM9_B	–
25	PD9	LCD_D9	SPI1_WP	–	–	PBUS_NCS	EPWM9_A	–
24	PD10	LCD_D10	CAP5	–	–	PBUS_NADV	EPWM8_B	–
23	PD11	LCD_D11	CAP4	I2S_DIN	–	PBUS_NWE	EPWM8_A	–
22	PD12	LCD_D12	CAP3	I2S_DOUT	–	PBUS_NOE	EPWM7_B	–
21	PD13	LCD_D13	CAP2	I2S_LRCK	–	CLK_OUT0	EPWM7_A	–
20	PD14	LCD_D14	CAP1	I2S_BCLK	–	PBUS_AD8	EPWM6_B	–
19	PD15	LCD_D15	CAP0	I2S_MCLK	–	PBUS_AD9	EPWM6_A	–
18	PD16	LCD_D16	PWM1_B	DMIC_CLK	UART2_TX	PBUS_AD10	EPWM5_B	–
17	PD17	LCD_D17	PWM2_A	DMIC_D0	UART2_RX	PBUS_AD11	EPWM5_A	–
16	PD18	LCD_D18	LVDS_D0N	DSI_D0N	–	PBUS_AD12	EPWM4_B	–
15	PD19	LCD_D19	LVDS_D0P	DSI_D0P	–	PBUS_AD13	EPWM4_A	–
14	PD20	LCD_D20	LVDS_D1N	DSI_D1N	–	PBUS_AD14	EPWM3_B	–

Table 5–3 D133BxS QFN68 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
13	PD21	LCD_D21	LVDS_D1P	DSI_D1P	–	PBUS_AD15	EPWM3_A	–
11	PD22	LCD_D22	LVDS_D2N	DSI_CKN	–	–	EPWM2_B	–
10	PD23	LCD_D23	LVDS_D2P	DSI_CKP	–	–	EPWM2_A	–
9	PD24	LCD_DCLK	LVDS_CKN	DSI_D2N	–	–	EPWM1_B	–
8	PD25	LCD_HS	LVDS_CKP	DSI_D2P	–	PWM2_B	EPWM1_A	–
7	PD26	LCD_VS	LVDS_D3N	DSI_D3N	–	PWM3_A	EPWM0_B	–
6	PD27	LCD_DE	LVDS_D3P	DSI_D3P	–	PWM3_B	EPWM0_A	–
GPIO E								
38	PE12	SPI2_CLK	PWM1_B	I2S_BCLK	DSPK1	–	–	–
39	PE13	SPI2_CS	PWM2_A	I2S_DOUT	DSPK0	–	–	–

5.3.2. D133CxS QFN88 Package Pin Description

Table 5–4 D133CxS QFN88 Package Pin Description

Pins	Definition	Signal Type	Function	Remark
RTC				
83	RTC_IO	OD	RTC wakeup output 32K clock output	OD output, with an external pullup resistor. The pullup voltage must be lower than 5 V.
84	RTC_VCOIN	POWER	–	Can be floating if power–off protection is not considered. The internal diode can be powered by a 3.3–V source. If connected externally for power supply, a RC must be connected for power–on delay (10 KΩ/ 0.1 uF).
85	RTC_XO	OUTPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
86	RTC_XI	INPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
SYS				
67	RESETN	INPUT	System Reset	Built in with a 30–kΩ pullup resistor and dethering filter which can be floating if not used. If an external capacitor is connected, the recommended load capacitance is less than 4.7 uF.
81	PLL_XO	OUTPUT	–	Connect with a 24–MHz crystal oscillator.
82	PLL_XI	INPUT	–	Connect with a 24–MHz crystal oscillator.
POWER				
15, 36, 69	For VCC33_IO	POWER	IO Voltage	3.3 –V power supply
70	LDO25	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
31	LDO18	POWER	Built–in LDO output	Used for internal PSRAM modules. If used otherwise, chip cooling must be considered. Connect with a 1–uF bypass capacitor
8, 30, 68	VDD11_SYS	POWER	Chip Core Voltage	1.1 V power supply. If the built–in LDO1x is used, chip cooling must be considered. Pin 68 is for LDO1x output.

Table 5–4 D133CxS QFN88 Package Pin Description (continued)

Pins	Definition	Signal Type	Function	Remark
89	GND	POWER	–	GND Copper full–cover connection via stitching for cooling.

Table 5–5 D133CB QFN88 Package Pin–mux

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
GPIO A								
71	PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX	–	PSADC0	CPU_NMI
72	PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX	–	PSADC1	DE_TE
73	PA2	GPADC2	–	I2C1_SCL	UART1_TX	–	PSADC2	UART2_CTS
74	PA3	GPADC3	–	I2C1_SDA	UART1_RX	–	PSADC3	UART2_RTS
75	PA4	GPADC4	–	CAN0_TX	UART2_TX	–	PSADC4	–
76	PA5	GPADC5	–	CAN0_RX	UART2_RX	–	PSADC5	RTC_32K
77	PA8	RTP_XP	–	I2C2_SCL	–	–	PSADC8	–
78	PA9	RTP_YP	–	I2C2_SDA	–	–	PSADC9	–
79	PA10	RTP_XN	IR_RX	–	–	–	PSADC10	JTAG_MS
80	PA11	RTP_YN	IR_TX	–	–	–	PSADC11	JTAG_CK
GPIO B								
55	PB0	SPI0_WP	SPI1_WP	–	UART4_TX	–	–	–
56	PB1	SPI0_MISO	SPI1_MISO	–	UART6_TX	–	–	–
57	PB2	SPI0_CS0	SPI1_CS0	–	UART6_RX	–	–	–
58	PB3	SPI0_HOLD	SPI1_HOLD	–	UART4_RX	–	–	–
59	PB4	SPI0_CLK	SPI1_CLK	–	UART6_RTS	–	–	–
60	PB5	SPI0_MOSI	SPI1_MOSI	–	UART4_RTS	UART6_CTS	–	–
61	PB6	SDC0_CMD	SPI2_CS	–	UART5_TX	–	–	–
62	PB7	SDC0_CLK	SPI2_MISO	–	UART5_RX	–	–	–
63	PB8	SDC0_D3	SPI2_MOSI	–	UART5_RTS	UART7_CTS	–	–
64	PB9	SDC0_D0	SPI2_CLK	–	UART7_RTS	–	–	–
65	PB10	SDC0_D1	SPI2_HOLD	–	UART7_TX	–	–	–
66	PB11	SDC0_D2	SPI2_WP	SPI0_CS1	UART7_RX	–	–	–
GPIO C								
1	PC0	SDC1_D1	–	I2C2_SCL	UART3_RTS	–	–	JTAG_MS
2	PC1	SDC1_D0	–	–	–	–	–	–
3	PC2	SDC1_CLK	–	–	–	–	–	UART0_TX
4	PC3	SDC1_CMD	–	–	–	–	–	–
5	PC4	SDC1_D3	–	I2C1_SCL	UART3_TX	–	–	UART0_RX
6	PC5	SDC1_D2	–	I2C1_SDA	UART3_RX	–	–	JTAG_CK
7	PC6	SDC1_DET	CAP0	I2C2_SDA	UART3_CTS	DE_TE	CLK_OUT3	–
GPIO D								
40	PD0	LCD_D0	SPI3_CLK	I2C0_SCL	UART0_TX	PBUS_AD0	EPWM11_B	–
39	PD1	LCD_D1	SPI3_CS0	I2C0_SDA	UART0_RX	PBUS_AD1	EPWM11_A	–
38	PD2	LCD_D2	SPI3_MOSI	I2C1_SCL	UART1_TX	PBUS_AD2	EPWM10_B	–

Table 5–5 D133CB QFN88 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
37	PD3	LCD_D3	SPI3_MISO	I2C1_SDA	UART1_RX	PBUS_AD3	EPWM10_A	–
35	PD4	LCD_D4	SPI1_CS0	I2C2_SCL	UART2_TX	PBUS_AD4	–	–
34	PD5	LCD_D5	SPI1_MISO	I2C2_SDA	UART2_RX	PBUS_AD5	–	–
33	PD6	LCD_D6	SPI1_MOSI	PWM0_A	DSPK0	PBUS_AD6	–	–
32	PD7	LCD_D7	SPI1_CLK	PWM0_B	DSPK1	PBUS_AD7	–	–
29	PD8	LCD_D8	SPI1_HOLD	PWM1_A	–	PBUS_CLK	EPWM9_B	–
28	PD9	LCD_D9	SPI1_WP	–	–	PBUS_NCS	EPWM9_A	–
27	PD10	LCD_D10	CAP5	–	–	PBUS_NADV	EPWM8_B	–
26	PD11	LCD_D11	CAP4	I2S_DIN	–	PBUS_NWE	EPWM8_A	–
25	PD12	LCD_D12	CAP3	I2S_DOUT	–	PBUS_NOE	EPWM7_B	–
24	PD13	LCD_D13	CAP2	I2S_LRCK	–	CLK_OUT0	EPWM7_A	–
23	PD14	LCD_D14	CAP1	I2S_BCLK	–	PBUS_AD8	EPWM6_B	–
22	PD15	LCD_D15	CAP0	I2S_MCLK	–	PBUS_AD9	EPWM6_A	–
21	PD16	LCD_D16	PWM1_B	DMIC_CLK	UART2_TX	PBUS_AD10	EPWM5_B	–
20	PD17	LCD_D17	PWM2_A	DMIC_D0	UART2_RX	PBUS_AD11	EPWM5_A	–
19	PD18	LCD_D18	LVDS_D0N	DSI_D0N	–	PBUS_AD12	EPWM4_B	–
18	PD19	LCD_D19	LVDS_D0P	DSI_D0P	–	PBUS_AD13	EPWM4_A	–
17	PD20	LCD_D20	LVDS_D1N	DSI_D1N	–	PBUS_AD14	EPWM3_B	–
16	PD21	LCD_D21	LVDS_D1P	DSI_D1P	–	PBUS_AD15	EPWM3_A	–
14	PD22	LCD_D22	LVDS_D2N	DSI_CKN	–	–	EPWM2_B	–
13	PD23	LCD_D23	LVDS_D2P	DSI_CKP	–	–	EPWM2_A	–
12	PD24	LCD_DCLK	LVDS_CKN	DSI_D2N	–	–	EPWM1_B	–
11	PD25	LCD_HS	LVDS_CKP	DSI_D2P	–	PWM2_B	EPWM1_A	–
10	PD26	LCD_VS	LVDS_D3N	DSI_D3N	–	PWM3_A	EPWM0_B	–
9	PD27	LCD_DE	LVDS_D3P	DSI_D3P	–	PWM3_B	EPWM0_A	–
GPIO E								
41	PE0	EMAC_RXD1	DVP_D0	PWM0_A	UART3_TX	–	–	–
42	PE1	EMAC_RXD0	DVP_D1	PWM0_B	UART3_RX	–	–	–
43	PE2	EMAC_CRS_DV	DVP_D2	–	UART4_TX	–	–	–
44	PE3	EMAC_REFCLK	DVP_D3	I2S_MCLK	UART4_RX	–	–	–
45	PE4	EMAC_TXD1	DVP_D4	–	UART5_TX	–	–	–
46	PE5	EMAC_TXD0	DVP_D5	–	UART5_RX	–	–	–
47	PE6	EMAC_TXC	DVP_D6	–	UART6_TX	–	–	–
48	PE7	EMAC_TXEN	DVP_D7	–	UART6_RX	–	–	–
49	PE8	EMAC_MDC	DVP_CK	–	UART7_TX	–	–	–
50	PE9	EMAC_MDIO	DVP_HS	–	UART7_RX	–	–	–
51	PE10	CLK_OUT2	DVP_VS	I2S_DIN	DMIC_CLK	–	–	–
52	PE11	CLK_OUT1	PWM1_A	I2S_LRCK	DMIC_D0	–	–	–
53	PE12	SPI2_CLK	PWM1_B	I2S_BCLK	DSPK1	–	–	–
54	PE13	SPI2_CS	PWM2_A	I2S_DOUT	DSPK0	–	–	–

Table 5–5 D133CB QFN88 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
USB								
87	PU0	USB_DM	–	UART0_RX	UART1_RX	–	–	–
88	PU1	USB_DP	–	UART0_TX	UART1_TX	–	–	–

5.3.3. D133ExS QFN100 Package Pin Description

Table 5–6 D133ExS/ D132ENS QFN100 Package Pin Description

Pins	Definition	Signal Type	Function	Remark
RTC				
93	RTC_IO	OD	RTC wakeup output 32K clock output	OD output, with an external pullup resistor. The pullup voltage must be lower than 5 V.
94	RTC_VCOIN	POWER	–	Can be floating if power–off protection is not considered. The internal diode can be powered by a 3.3–V source. If connected externally for power supply, a RC must be connected for power–on delay (10 KΩ/ 0.1 uF).
95	RTC_XO	OUTPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
96	RTC_XI	INPUT	–	Connected with a 32.768–KHz crystal oscillator which can be floating if RTC is not used.
SYSTEM				
75	RESETN	INPUT	System Reset	Built in with a 30kΩ pullup resistor and dithering filter which can be floating if not used. If an external capacitor is connected, the recommended load capacitance is less than 4.7 uF.
91	PLL_XO	OUTPUT	–	Connect with a 24–MHz crystal oscillator.
92	PLL_XI	INPUT	–	Connect with a 24–MHz crystal oscillator.
POWER				
19, 36, 77, 99	For VCC33_IO	POWER	IO Voltage	3.3 –V power supply
78	LDO25	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
35	LDO18	POWER	Built–in LDO output	Used for internal PSRAM modules. If used otherwise, chip cooling must be considered. Connect with a 1–uF bypass capacitor.
7, 34, 76	VDD11_SYS	POWER	Chip Core Voltage	1.1 V power supply. If the built–in LDO1x is used, chip cooling must be considered. Pin 76 is for LDO1x output.
101	GND	POWER	–	GND Copper full–cover connection via stitching for cooling.

Table 5–7 D133ExS/ D132ENS QFN100 Package Pin Description

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
GPIO A								
79	PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX	–	PSADC0	CPU_NMI
80	PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX	–	PSADC1	DE_TE
81	PA2	GPADC2	–	I2C1_SCL	UART1_TX	–	PSADC2	UART2_CTS
82	PA3	GPADC3	–	I2C1_SDA	UART1_RX	–	PSADC3	UART2_RTS

Table 5–7 D133ExS/ D132ENS QFN100 Package Pin Description (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
83	PA4	GPADC4	–	CAN0_TX	UART2_TX	–	PSADC4	–
84	PA5	GPADC5	–	CAN0_RX	UART2_RX	–	PSADC5	RTC_32K
85	PA6	GPADC6	–	CAN1_TX	UART3_TX	–	PSADC6	–
86	PA7	GPADC7	–	CAN1_RX	UART3_RX	–	PSADC7	–
87	PA8	RTP_XP	–	I2C2_SCL	–	–	PSADC8	–
88	PA9	RTP_YP	–	I2C2_SDA	–	–	PSADC9	–
89	PA10	RTP_XN	IR_RX	–	–	–	PSADC10	JTAG_MS
90	PA11	RTP_YN	IR_TX	–	–	–	PSADC11	JTAG_CK
GPIO B								
63	PB0	SPI0_WP	SPI1_WP	–	UART4_TX	–	–	–
64	PB1	SPI0_MISO	SPI1_MISO	–	UART6_TX	–	–	–
65	PB2	SPI0_CS0	SPI1_CS0	–	UART6_RX	–	–	–
66	PB3	SPI0_HOLD	SPI1_HOLD	–	UART4_RX	–	–	–
67	PB4	SPI0_CLK	SPI1_CLK	–	UART6_RTS	–	–	–
68	PB5	SPI0_MOSI	SPI1_MOSI	–	UART4_RTS	UART6_CTS	–	–
69	PB6	SDC0_CMD	SPI2_CS	–	UART5_TX	–	–	–
70	PB7	SDC0_CLK	SPI2_MISO	–	UART5_RX	–	–	–
71	PB8	SDC0_D3	SPI2_MOSI	–	UART5_RTS	UART7_CTS	–	–
72	PB9	SDC0_D0	SPI2_CLK	–	UART7_RTS	–	–	–
73	PB10	SDC0_D1	SPI2_HOLD	–	UART7_TX	–	–	–
74	PB11	SDC0_D2	SPI2_WP	SPI0_CS1	UART7_RX	–	–	–
GPIO C								
100	PC0	SDC1_D1	–	I2C2_SCL	UART3_RTS	–	–	JTAG_MS
1	PC1	SDC1_D0	–	–	–	–	–	–
2	PC2	SDC1_CLK	–	–	–	–	–	UART0_TX
3	PC3	SDC1_CMD	–	–	–	–	–	–
4	PC4	SDC1_D3	–	I2C1_SCL	UART3_TX	–	–	UART0_RX
5	PC5	SDC1_D2	–	I2C1_SDA	UART3_RX	–	–	JTAG_CK
6	PC6	SDC1_DET	CAP0	I2C2_SDA	UART3_CTS	DE_TE	CLK_OUT3	–
8	PC7	–	CAP1	–	–	–	–	–
9	PC8	SPI3_CLK	CAP2	CAN0_TX	UART4_TX	–	–	–
10	PC9	SPI3_CS0	CAP3	CAN0_RX	UART4_RX	–	–	–
11	PC10	SPI3_MOSI	CAP4	CAN1_TX	UART5_TX	–	–	–
12	PC11	SPI3_MISO	CAP5	CAN1_RX	UART5_RX	–	–	–
GPIO D								
44	PD0	LCD_D0	SPI3_CLK	I2C0_SCL	UART0_TX	PBUS_AD0	EPWM11_B	–
43	PD1	LCD_D1	SPI3_CS0	I2C0_SDA	UART0_RX	PBUS_AD1	EPWM11_A	–
42	PD2	LCD_D2	SPI3_MOSI	I2C1_SCL	UART1_TX	PBUS_AD2	EPWM10_B	–
41	PD3	LCD_D3	SPI3_MISO	I2C1_SDA	UART1_RX	PBUS_AD3	EPWM10_A	–
40	PD4	LCD_D4	SPI1_CS0	I2C2_SCL	UART2_TX	PBUS_AD4	–	–

Table 5–7 D133ExS/ D132ENS QFN100 Package Pin Description (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
39	PD5	LCD_D5	SPI1_MISO	I2C2_SDA	UART2_RX	PBUS_AD5	–	–
38	PD6	LCD_D6	SPI1_MOSI	PWM0_A	DSPK0	PBUS_AD6	–	–
37	PD7	LCD_D7	SPI1_CLK	PWM0_B	DSPK1	PBUS_AD7	–	–
33	PD8	LCD_D8	SPI1_HOLD	PWM1_A	–	PBUS_CLK	EPWM9_B	–
32	PD9	LCD_D9	SPI1_WP	–	–	PBUS_NCS	EPWM9_A	–
31	PD10	LCD_D10	CAP5	–	–	PBUS_NADV	EPWM8_B	–
30	PD11	LCD_D11	CAP4	I2S_DIN	–	PBUS_NWE	EPWM8_A	–
29	PD12	LCD_D12	CAP3	I2S_DOUT	–	PBUS_NOE	EPWM7_B	–
28	PD13	LCD_D13	CAP2	I2S_LRCK	–	CLK_OUT0	EPWM7_A	–
27	PD14	LCD_D14	CAP1	I2S_BCLK	–	PBUS_AD8	EPWM6_B	–
26	PD15	LCD_D15	CAP0	I2S_MCLK	–	PBUS_AD9	EPWM6_A	–
25	PD16	LCD_D16	PWM1_B	DMIC_CLK	UART2_TX	PBUS_AD10	EPWM5_B	–
24	PD17	LCD_D17	PWM2_A	DMIC_D0	UART2_RX	PBUS_AD11	EPWM5_A	–
23	PD18	LCD_D18	LVDS_D0N	DSI_D0N	–	PBUS_AD12	EPWM4_B	–
22	PD19	LCD_D19	LVDS_D0P	DSI_D0P	–	PBUS_AD13	EPWM4_A	–
21	PD20	LCD_D20	LVDS_D1N	DSI_D1N	–	PBUS_AD14	EPWM3_B	–
20	PD21	LCD_D21	LVDS_D1P	DSI_D1P	–	PBUS_AD15	EPWM3_A	–
18	PD22	LCD_D22	LVDS_D2N	DSI_CKN	–	–	EPWM2_B	–
17	PD23	LCD_D23	LVDS_D2P	DSI_CKP	–	–	EPWM2_A	–
16	PD24	LCD_DCLK	LVDS_CKN	DSI_D2N	–	–	EPWM1_B	–
15	PD25	LCD_HS	LVDS_CKP	DSI_D2P	–	PWM2_B	EPWM1_A	–
14	PD26	LCD_VS	LVDS_D3N	DSI_D3N	–	PWM3_A	EPWM0_B	–
13	PD27	LCD_DE	LVDS_D3P	DSI_D3P	–	PWM3_B	EPWM0_A	–
GPIO E								
45	PE0	EMAC_RXD1	DVP_D0	PWM0_A	UART3_TX	–	–	–
46	PE1	EMAC_RXD0	DVP_D1	PWM0_B	UART3_RX	–	–	–
47	PE2	EMAC_CRS_DV	DVP_D2	–	UART4_TX	–	–	–
48	PE3	EMAC_REFCLK	DVP_D3	I2S_MCLK	UART4_RX	–	–	–
49	PE4	EMAC_TXD1	DVP_D4	–	UART5_TX	–	–	–
50	PE5	EMAC_TXD0	DVP_D5	–	UART5_RX	–	–	–
51	PE6	EMAC_TXC	DVP_D6	–	UART6_TX	–	–	–
52	PE7	EMAC_TXEN	DVP_D7	–	UART6_RX	–	–	–
53	PE8	EMAC_MDC	DVP_CK	–	UART7_TX	–	–	–
54	PE9	EMAC_MDIO	DVP_HS	–	UART7_RX	–	–	–
55	PE10	CLK_OUT2	DVP_VS	I2S_DIN	DMIC_CLK	–	–	–
56	PE11	CLK_OUT1	PWM1_A	I2S_LRCK	DMIC_D0	–	–	–
57	PE12	SPI2_CLK	PWM1_B	I2S_BCLK	DSPK1	–	–	–
58	PE13	SPI2_CS	PWM2_A	I2S_DOUT	DSPK0	–	–	–
59	PE14	SPI2_MOSI	I2S_MCLK	I2C0_SCK	UART6_TX	–	–	–
60	PE15	SPI2_MISO	PWM2_B	I2C0_SDA	UART6_RX	–	–	–

Table 5–7 D133ExS/ D132ENS QFN100 Package Pin Description (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
61	PE16	SPI2_HOLD	PWM3_A	–	UART7_TX	–	–	–
62	PE17	SPI2_WP	PWM3_B	–	UART7_RX	–	–	–
USB								
97	PU0	USB_DM	–	UART0_RX	UART1_RX	–	–	–
98	PU1	USB_DP	–	UART0_TX	UART1_TX	–	–	–

5.4. Pin Description

Pin/Signal Name	Description	Signal Type
SYSTEM		
RESETN	Reset pin	I
PLL_XI	24 –MHz crystal oscillator input capacitance	AI
PLL_XO	24 MHz crystal oscillator	AO
RTC		
RTC_IO	RTC 唤醒信号或 32.768 KHz 时钟输出	OD
RTC_VCOIN	Button–cell power source for RTC	P
RTC_XO	32.768 KHz crystal oscillator	AO
RTC_XI	32.768 –KHz crystal oscillator input capacitance	AI
USB		
USB_DM	USB Data Minus	AI/O
USB_DP	USB Data Positive	AI/O
RTP		
RTP_XP	RTP X positive	AI
RTP_YP	RTP Y positive	AI
RTP_XN	RTP X negative	AI
RTP_YN	RTP Y negative	AI
ADC，x = 0~7		
GPADCx	General–purpose analog input	AI
ADC，x = 0~11		
PSADCx	General–purpose analog input	AI
EMAC		
EMAC_RXD1	RMII receive data 1	I
EMAC_RXD0	RMII receive data 0	I
EMAC_CRS_DV	RMII receive data valid	I
EMAC_REFCLK	RMII reference clock	I
EMAC_TXD1	RMII transmit data 1	O
EMAC_TXD0	RMII transmit data 0	O
EMAC_TXC	RMII transmit clock	O
EMAC_TXEN	RMII transmit enable	O
EMAC_MDC	RMII management data clock	I/O
EMAC_MDIO	RMII management data input/output	I/O

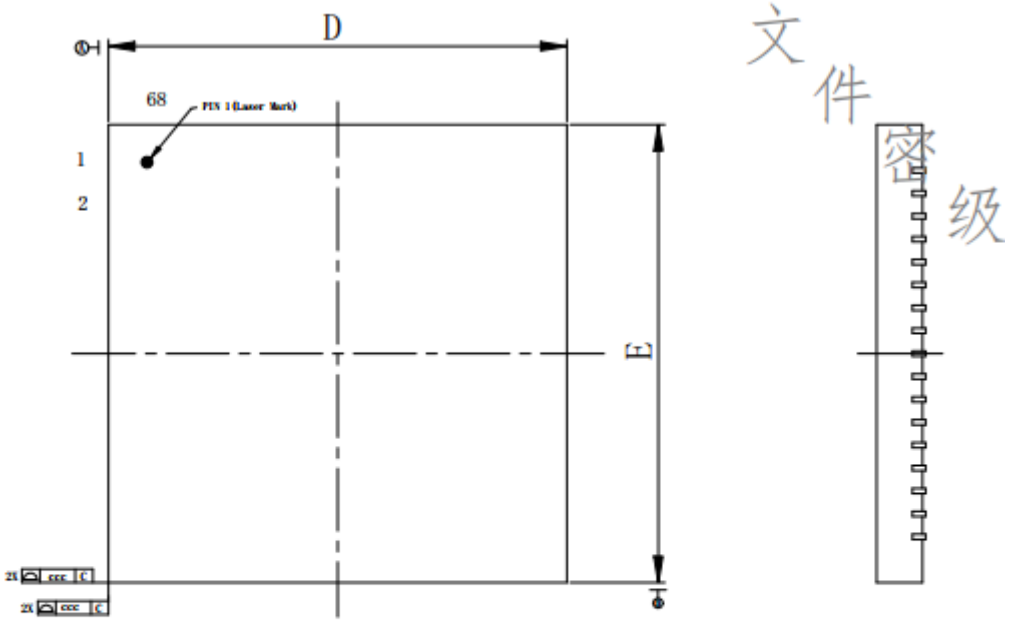
Pin/Signal Name	Description	Signal Type
CLK_OUTx	For configuration of 25 MHz clock output, x = 0~3	O
PWM，x = 0~3		
PWMx_A	PWMx Channel A	O
PWMx_B	PWMx Channel B	O
EPWM，x = 0~11		
EPWMx_A	EPWMx Channel A	O
EPWMx_B	EPWMx Channel B	O
CAP，x = 0~5		
CAPx	CAP input capture or PWM output	I/O
SPI，x = 0~3		
SPIx_HOLD	SPIx hold signal, valid for low-level voltage	I/O
SPIx_WP	SPIx write protection, valid for low-level voltage	I/O
SPIx_CS	SPIx chip select signal, valid for low-level voltage.	I/O
SPIx_CLK	SPIx clock signal	I/O
SPIx_MOSI	SPIx master out slave in	I/O
SPIx_MISO	SPIx master in slave out	I/O
UART，x = 0~7		
UARTx_TX	UARTx data transmission	O
UARTx_RX	UARTx data reception	I
UARTx_CTS	UARTx confirmed transmission	I
UARTx_RTS	UARTx requested transmission	O
I2C，x = 0~2		
I2Cx_SCL	I2C serial clock line	I/O
I2Cx_SDA	I2Cx serial data line	I/O
CAN		
CAN0_TX	CAN0 data transmission, connected with a CAN transceiver	O
CAN0_RX	CAN0 data reception, connected with a CAN receiver	I
CAN1_TX	CAN1 data t, connected with a CAN receiver	O
CAN1_RX	CAN1 data reception, connected with a CAN receiver	I
CIR		
IR_TX	Infrared data transmit	O
IR_RX	Infrared data receive	I
I2S		
I2S_MCLK	I2Sx master clock	O
I2S_LRCK	I2Sx left/right clock	I/O
I2S_BCLK	I2Sx bit clock	I/O
I2S_DOUT	I2Sx data output	O
I2S_DIN	I2Sx data input	I
DSPK		
DSPK0	Speaker signal output channel 0	O
DSPK1	Speaker signal output channel 1	O
DMIC		

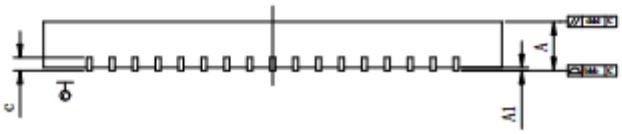
Pin/Signal Name	Description	Signal Type
DMIC_CLK	PDM clock signal	O
DMIC_D0	PDM data signal	I/O
SDC，x = 0~1		
SDCx_CMD	SDC0 command signal	I/O
SDCx_CLK	SDC0 clock signal	O
SDCx_D[3:0]	SDC0 data output/input	I/O
LCD		
LCD_D[23:0]	LCD data output	O
LCD_DCLK	LCD clock data signal	O
LCD_HS	LCD horizontal synchronization	O
LCD_VS	LCD vertical synchronization	O
LCD_DE	LCD data enable	O
LVDS		
LVDS_CKN	LVDSx clock negative	AO
LVDS_CKP	LVDSx clock positive	AO
LVDS_D0N	LVDSx data 0 negative	AO
LVDS_D0P	LVDSx data 0 positive	AO
LVDS_D1N	LVDSx data 1 negative	AO
LVDS_D1P	LVDSx data 1 positive	AO
LVDS_D2N	LVDSx data 2 negative	AO
LVDS_D2P	LVDSx data 2 positive	AO
LVDS_D3N	LVDSx data 3 negative	AO
LVDS_D3P	LVDSx data 3 positive	AO
MIPI DSI		
DSI_CKN	MIPI DSI clock negative	AO
DSI_CKP	MIPI DSI clock positive	AO
DSI_D0N	MIPI DSI data 0 negative	AO
DSI_D0P	MIPI DSI data 0 positive	AO
DSI_D1N	MIPI DSI data 1 negative	AO
DSI_D1P	MIPI DSI data 1 positive	AO
DSI_D2N	MIPI DSI data 2 negative	AO
DSI_D2P	MIPI DSI data 2 positive	AO
DSI_D3N	MIPI DSI data 3 negative	AO
DSI_D3P	MIPI DSI data 3 positive	AO
DVP		
DVP_CK	DVP clock	I
DVP_HS	DVP	I
DVP_VS	DVP vertical synchronization	I
DVP_D[7:0]	DVP data input	I
PBUS		
PBUS_CLK	PBUS external clock signal	O
PBUS_NCS	PBUS chip select signal, valid for low-level voltage	O

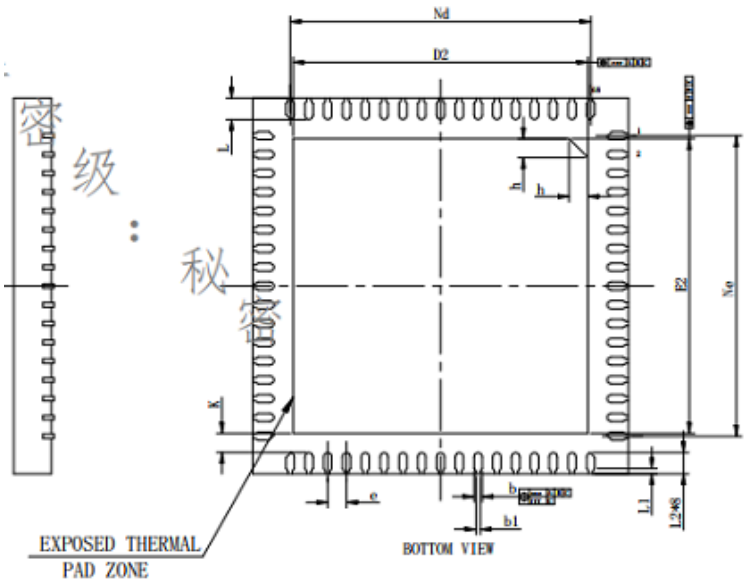
Pin/Signal Name	Description	Signal Type
PBUS_NADV	PBUS address valid signal, valid for low–level voltage	O
PBUS_NWE	PBUS read/ write control signal, low–level voltage for write, high–level voltage for read.	O
PBUS_NOE	PBUS output enabling signal, valid for low–level voltage	O
PBUS_AD[15:0]	PBUS Address/Data Bus	I/O

5.5. Package Size

5.5.1. D133BxS QFN68

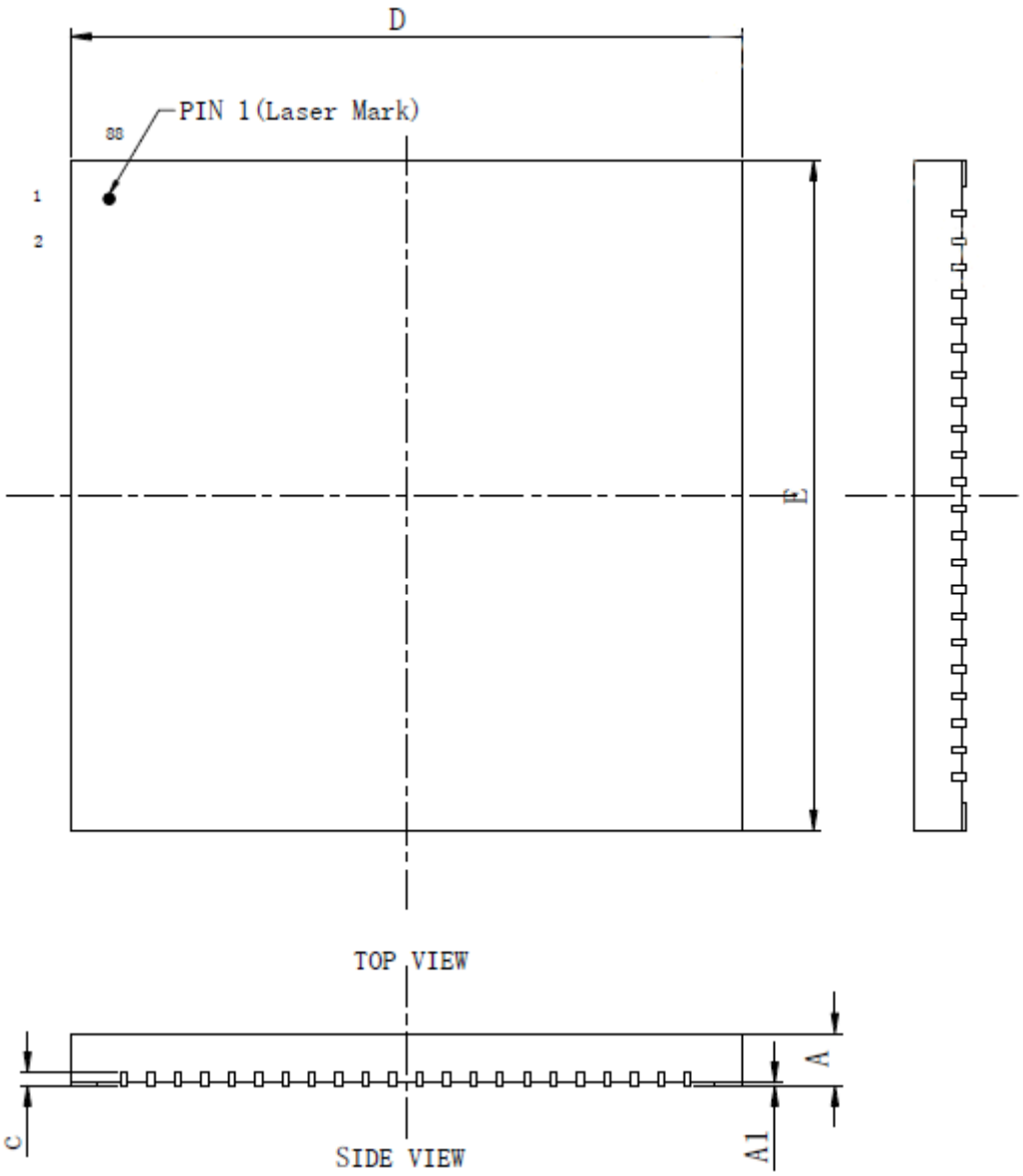


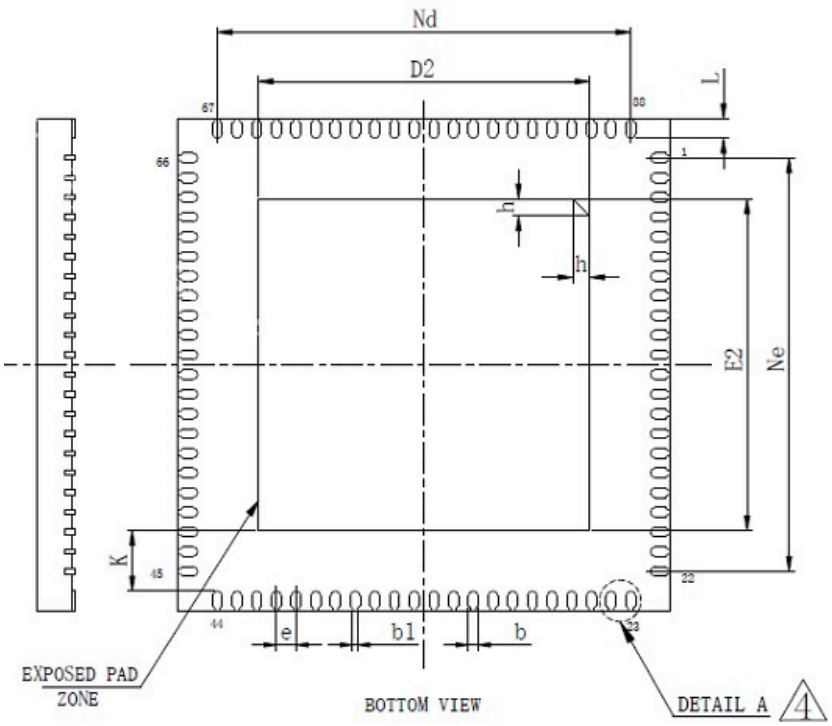




SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	①
	0.85	0.90	0.95	②
A1	—	0.02	0.05	
b	0.10	0.15	0.20	
b1	0.08REF			
c	0.18	0.20	0.25	
D	6.90	7.00	7.10	
D2	5.39	5.49	5.59	
e	0.35BSC			
Nd	5.60BSC			
E	6.90	7.00	7.10	
E2	5.39	5.49	5.59	
Ne	5.60BSC			
L	0.35	0.40	0.45	
L1	0.10REF			
L2	0.30	0.40	0.50	③
K	0.20	--	--	
h	0.30	0.35	0.40	

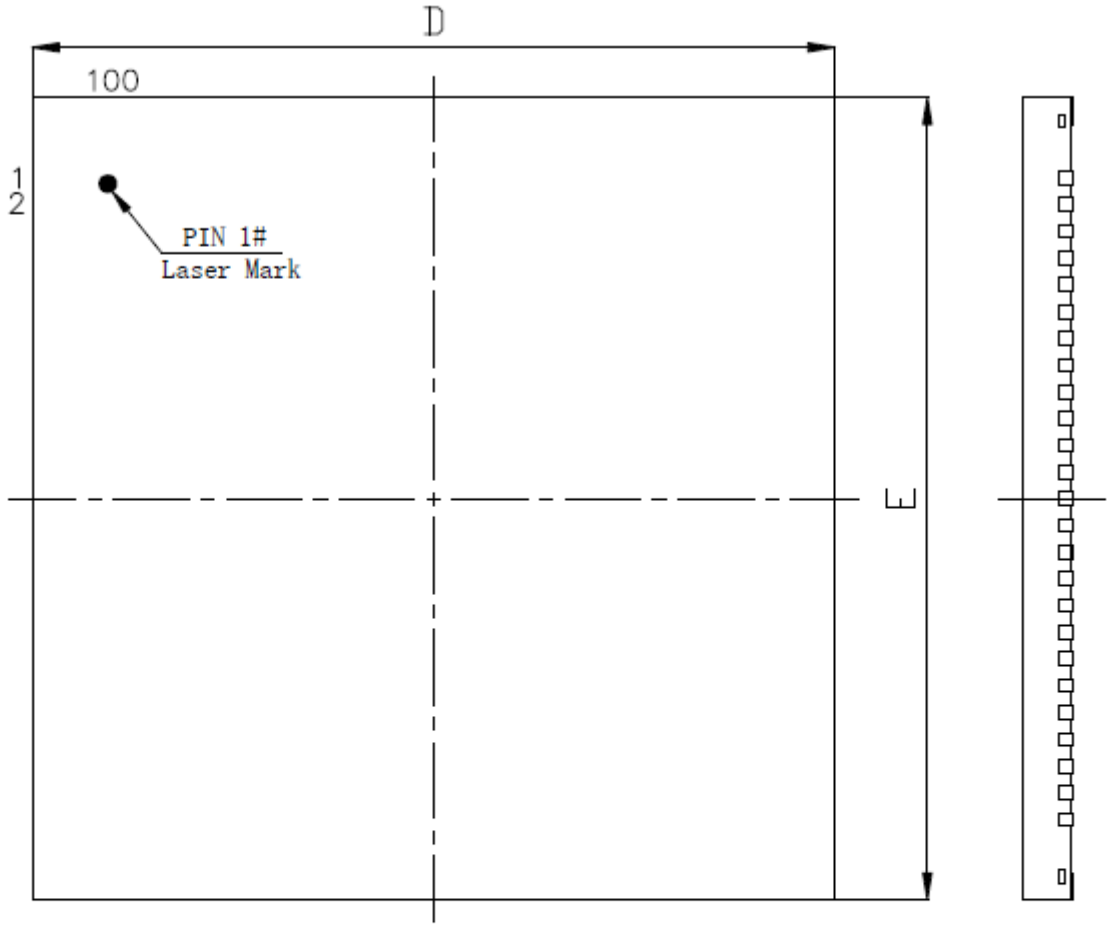
5.5.2. D133CxS QFN88



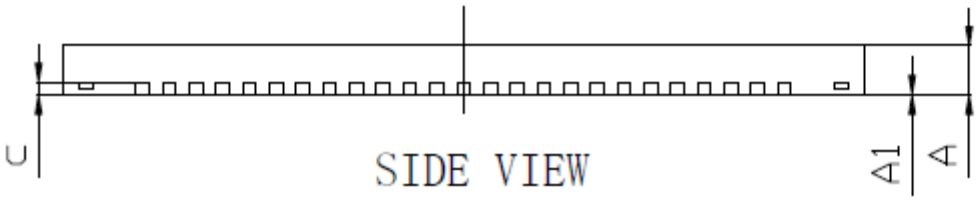


SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	1
	0.80	0.85	0.90	
	0.85	0.90	0.95	2
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.10REF			2
c	0.18	0.20	0.25	
D	9.90	10.00	10.10	
D2	6.64	6.74	6.84	
e	0.40BSC			
Nd	8.40REF			
E	9.90	10.00	10.10	
E2	6.64	6.74	6.84	
Ne	8.40REF			
L	0.30	0.40	0.50	
K	0.20	-	-	
h	0.30	0.35	0.40	

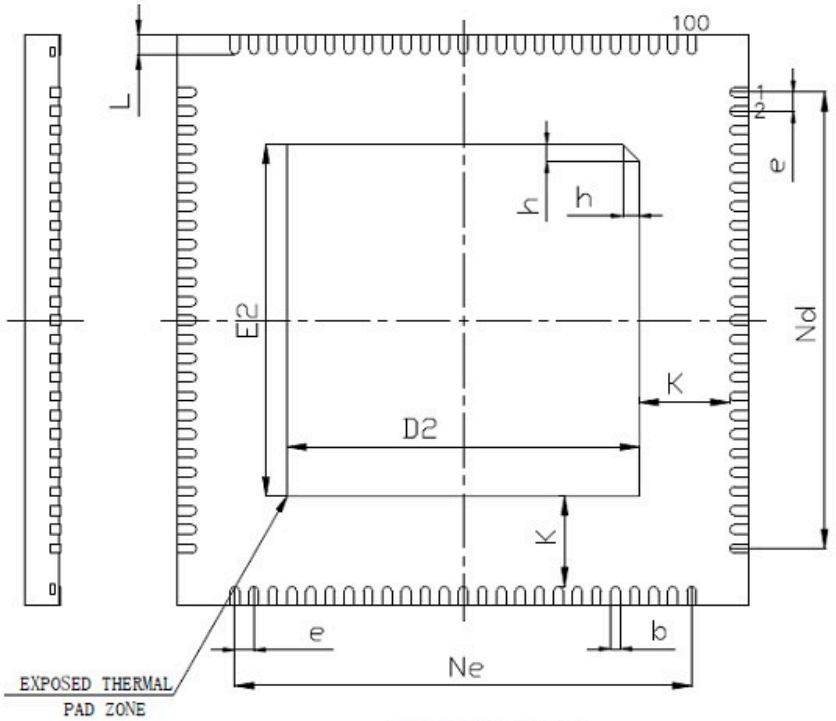
5.5.3. D133ExS QFN100



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.80	0.85	0.90	△
	0.70	0.75	0.80	
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
c	0.203REF			
D	11.90	12.00	12.10	
D2	7.30	7.40	7.50	
e	0.40BSC			
Ne	9.60BSC			
Nd	9.60BSC			
E	11.90	12.00	12.10	
E2	7.30	7.40	7.50	
L	0.35	0.40	0.45	
h	0.30	0.35	0.40	
K	1.90REF			