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D12x Datasheet

Version 1.5

Revision Date: 2025-01-09

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Revision History

Version	Section	Description
V1.3	–	Aligned styles.
	Functional Features	Updated fucntion descriptions.
	Product Information	Added D122BCV Sip 16MB PSRAM.
V1.4	Power–on/Power–off Sequence and Reset	Added the following description: • The rising edge working at 3.3V shall be detected after 150 us.
V1.5	Product Information	Added the following changes: • Added D121BCV. • Added D123BAV/ D123BBV /D123BCV with CAN and external 24M crystal oscillator. • Deleted D122BAV/ D122BBV/ D122BCV with CAN and built–in OSC24M. • Enabled the PA8~PA11 RTP pins for ADC function.

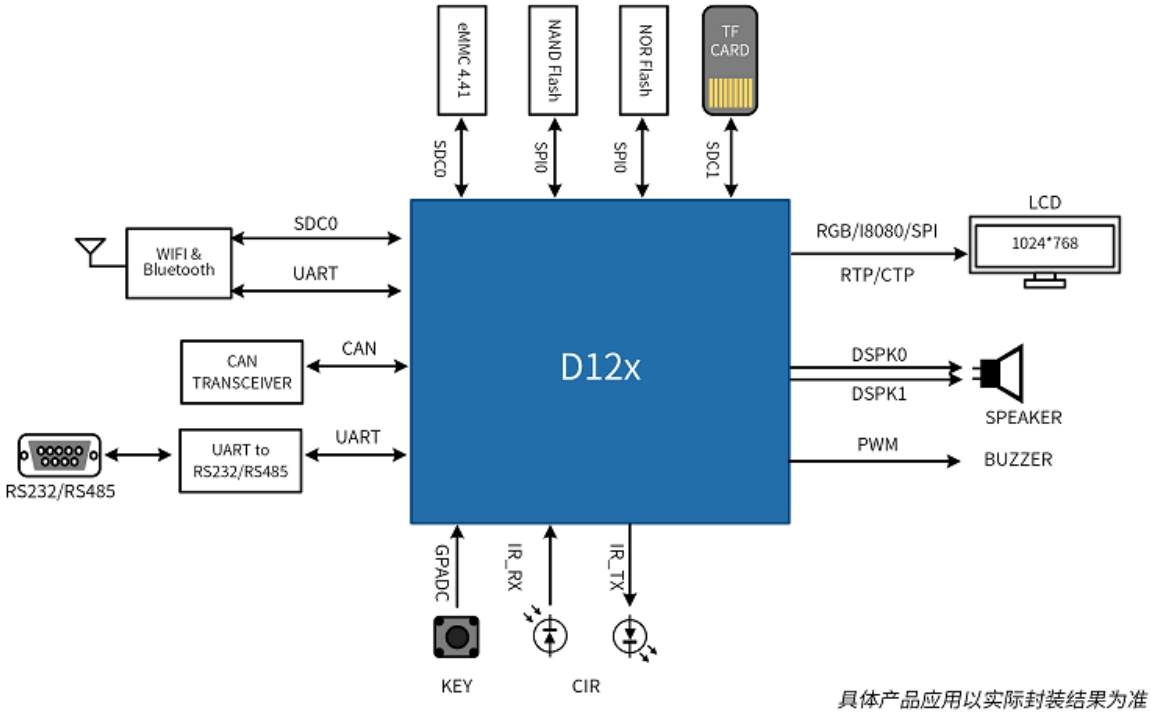
Contents

1. Introduction

D12x is a domestically independent MCU family based on RISC-V with high performance, industrial full-HD and smart control. Equipped with a powerful 2D image accelerator, PNG decoder, JPEG decoder engine and various display interfaces, D12x is of high reliability and openness and provides wide industrial temperatures. It can be widely applied in industrial automation control, serial screen and other smart industry and smart home fields.

Display out	Processor	Memory
RGB 1024x768	RISC-V 32-bit CPU	128/ 64/ 32 Mb PSRAM
I8080	I-Cache 32KB	eMMC I/F
QSPI	D-Cache 16KB	QSPI I/F

Multimedia	System	Connectivity	
Display Engine 1024x768@60fps	SPI ENC	DSPK 2ch	SDMC x 2
2D Graphics Engine	DMA	UART x 4	QSPI x 2
JPEG Decoder	Temp. Sensor	CAN x 2	CIR
PNG Decoder	eFuse	RTP	I2C x 2
	Watchdog	ADC 6ch	PWM 4ch



具体产品应用以实际封装结果为准

2. Functional Features

- **CPU Core**
  - E907 single–core processor, RV32IMAFC instruction set, 400 MHz@1.1V
  - 32–KB L1 instruction cache and 16–KB L1 data cache
  - Physical Memory Protection
  - Standard CLINT and PLIC interrupt controllers
  - Machine and User Mode
  - Standard 2–wire JTAG debug interface
- **Boot**
  - Default boot sequence: SD Card (SDMC1) → NOR (SPI0) → NAND (SPI0) → eMMC (SDMC0)
  - Default boot device configuration available by burning eFuse
- **System Safety**
  - SPI NAND/SPI NOR decode algorithms for SPI ENC
  - Data Check Engine (DCE) performs data integrity checks using two different algorithms: the CRC–32 polynomial method and the checksum method.
  - Embedded 512–bit eFuse for SID, of which 128 bits are for user customization
- **On-chip Memory**
  - 32 –KB BROM
  - 32 KB SRAM
  - PSRAM has the following specification choices:
    - 128 Mb DDR, with a 16–bit bus width and a maximum frequency of 200 MHz
    - 64 Mb DDR, with a 16–bit bus width and a maximum frequency of 200 MHz
    - 32 Mb, 8–bit width, with up to 200–MHz DDR
  - Spread spectrum supported for PSRAM clock
- **Memory Interfaces**
  - SPI NAND Flash / SPI NOR Flash supported for QSPI
    - Standard, dual SPI and quad SPI supported
    - Up to 100–MHz SDR for IO
  - Two sets of eMMC 4.41/ SD 2.0/ SDIO 2.0
    - 4–bit SDR25/ SDR50/ DDR50 data transfer for eMMC
    - SDR25/ SDR50 supported for SD cards
    - Up to 50–MHz of DDR for IO with 3.3 V voltage support only
- **Graph Engine**
  - Disply Engine (DE)
    - One UI layer with up to 1024x768@60fps
    - Dithering, Gamma and Color Correction Matrix adjustable
  - Graph Engine
    - 2D image acceleration, with a performance of up to 1080P@60fps
    - Horizontal and vertical flip support with 90/180/270–degree rotation angles
    - Rotation at any angle and scan order support for RGB graphs
    - 1/16x ~ 16x scaling scope support with bilinear filtering algorithm
    - Command queue
  - VE CODEC
    - JPEG decoder, with the highest performance of 720P@60fps
    - PNG decoder, with the highest performance of 720P@60fps
- **Display Interfaces**
  - 24–bit parallel port RGB, with the highest performance of 1024 x 768@60fps
  - SRGB/ I8080/ QSPI interfaces
  - Spread spectrum
- **Audio Interface**
  - Two digital PWM outpus (DSPK) with support for two single–ended L/R channels and one differential mono channel
- **General Interface**

- Two QSPI interfaces for standard, dual SPI and quad SPI, configurable as Master
- Four UART ports, supporting 2–wire/ 3–wire/ 4–wire interfaces that compatible with industry standard 16550
- Two 7–bit and 10–bit I2C interfaces with up to 400 Kb/s of addressing rate
- Two CAN modules with support for CAN2.0A and CAN2.0, and up to 1 Mbps of programmable comminicatable speed
- One CIR that supports infrared input and output
- Five GPIO interfaces with a total of 60 IOs individually configurable
  - Resistor options: no pullup, pullup 33KΩ, pulldown 33KΩ
  - Eight output driver levels available
  - Two–level dithering and interrupts for inputs
  - Bit operation support for data output registers

- **Timer**
  - GTC Generic Timers
    - 52–bit timer for system heartbeat clock with over 35 years of clocking cycle
    - Pause or Resume timer configurable in debug mode
  - WDOG
    - Interrupt and reset mode with configurable timeout period from 1ms to 37 hours
    - Pause or Resume timer configurable in debug mode
    - Firmware write protection
  - PWM
    - Built–in 16–bit counter
    - Support up to four independent PWM channels or two complementary PWM channels

- **Analog**
  - Built–in 6–channel 12–bit GPADC with a maximum sampling rate of 1 Msps.
  - Integrated resistive touch pannel (RTP), which can be used for ADC functions if RTP is not used

- **Clock and Power Management**
  - External Clock Source
    - Built–in ± 2% OSC24M. Crystal–free design is supported.
    - External crystal is supported, using an external 24M crystal oscillator. Crystal accuracy depends the crystal used.
  - Four built–in PLLs in CMU:
    - PLL_INT0 for CPU only
    - PLL_INT1 for BUS, internal modules, and low speed interface units
    - PLL_FRA0 for memory interfaces with the spread spectrum feature
    - PLL_FRA2 for display output modules with the spread spectrum feature
  - Three built–in LDO modules for SYSCFG:
    - LDO25 (2.5 V 100 mA), for power supply of system reset boot, ADC and eFuse
    - Built–in LDO18 (1.8 V 100 mA) for power supply of PSRAM IO and PSRAM
    - LDO1x (1.0 ~ 1.375 V 200 mA, 25 mV for each), for IO power supply of VDD_SYS modules
  - Built–in THS for high and low temperature interrupt alarms and over–temperature protection

3. Product Information

Table 3–1 Product

Model	Feature	Package	Temperature
D121BCV	16 MB PSRAM, without CAN	QFN68, 7 x 7 x 0.85 mm, with an interval of 0.35 mm	–20 to +105℃
D121BBV	8 MB PSRAM, without CAN	QFN68, 7 x 7 x 0.85 mm, with an interval of 0.35 mm	–20 to +105℃
D121BAV	4 MB PSRAM, without CAN interface	QFN68, 7 x 7 x 0.85 mm, with an interval of 0.35 mm	–20 to +105℃
D123BCV	16 MB PSRAM, with CAN interface	QFN68, 7 x 7 x 0.85 mm, with an interval of 0.35 mm	–20 to +105℃
D123BBV	8 MB PSRAM, with CAN interface	QFN68, 7 x 7 x 0.85 mm, with an interval of 0.35 mm	–20 to +105℃
D123BAV	4 MB PSRAM, with CAN interface	QFN68, 7 x 7 x 0.85 mm, with an interval of 0.35 mm	–20 to +105℃

Table 3–2 Product Comparison

Item	D121BCV	D121BBV	D121BAV	D123BCV	D123BBV	D123BAV
CPU	E907 400MHz@1.1V	E907 400MHz@1.1V	E907 400MHz@1.1V	E907 400MHz@1.1V	E907 400MHz@1.1V	E907 400MHz@1.1V
Memory	32 KB SRAM 16 MB PSRAM	32 KB SRAM 8 MB PSRAM	32 KB SRAM 4 MB PSRAM	32 KB SRAM 16 MB PSRAM	32 KB SRAM 8 MB PSRAM	32 KB SRAM 4 MB PSRAM
Safety	Support	Support	Support	Support	Support	Support
Clock	Built–in OSC	Built–in OSC	Built–in OSC	External crystal oscillator	External crystal oscillator	External crystal oscillator
RGB	x 1	x 1	x 1	x 1	x 1	x 1
RTP	x 1	x 1	x 1	x 1	x 1	x 1
SD 2.0	x 1	x 1	x 1	x 1	x 1	x 1
eMMC 4.41/ SDIO 2.0	x 1	x 1	x 1	x 1	x 1	x 1
DSPK	x 2	x 2	x 2	x 2	x 2	x 2
SPI	x 2	x 2	x 2	x 2	x 2	x 2
UART	x 4	x 4	x 4	x 4	x 4	x 4
I2C	x 2	x 2	x 2	x 2	x 2	x 2
CAN	–	–	–	x 2	x 2	x 2
CIR	x 1	x 1	x 1	x 1	x 1	x 1
PWM	x 2 (4 ch)	x 2 (4 ch)	x 2 (4 ch)	x 2 (4 ch)	x 2 (4 ch)	x 2 (4 ch)
ADC	x 1 (6 ch)	x 1 (6 ch)	x 1 (6 ch)	x 1 (4 ch)	x 1 (4 ch)	x 1 (4 ch)

4. Electrical Features

4.1. Operating Conditions

4.1.1. Maximum Values

Symbol	Description	Minimum	Maximum	Unit
Tstg	Storage temperature	–40	125	℃
For VCC33_IO	GPIO Power	–0.3	3.6	V
VDD11_SYS	Kernel and system power supply	–0.3	1.32	V
Iio	IO input/output current	–55	60	mA

4.1.2. Recommended Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit
Tj	Junction temperature	–20	–	105	℃
Ta	Ambient temperature	–20	–	85	℃
For VCC33_IO	GPIO Power	3.0	3.3	3.6	V
VDD11_SYS	Kernel and system power supply	0.99	1.1	1.21	V

4.2. Power–on/Power–off Sequence and Reset

4.2.1. Power–on/Power–off Sequence

There is no power–on and power–off sequence requirement for VCC33_IO, VDD11_SYS and LDO18. The rising edge working at VCC33_IO shall be detected after 150 us.

4.2.2. Reset Source

When any of the following reset conditions is met, the chip will reset:

- SYS power–on reset: a reset is triggered when VCC33_IO and VDD11_SYS are powered on. The system automatically releases the reset within 10 ms after power on.
- External pin reset: a reset is triggered when the RESETN pin is driven low for over 2 ms.
- Debugger reset: a reset is immediately triggered upon receiving the RESET signal from JTAG IO.
- Watchdog reset: when the reset is enabled, a reset is immediately triggered when the configured timeout reset conditions are met in WDOG.
- Over–temperature reset: when the reset is enabled, a reset is immediately triggered when the temperature is higher than the configured temperature in THS.

4.3. Built–in LDO Electrical Features

4.3.1. LDO25

The built–in LDO25 is used for power supply of analog subsystems and GPADC/ eFuse. Voltage is configurable. LDO25 is the referenced voltage for GPADC and Its electrical characteristics are as follows:

Symbol	Description	Minimum	Typical	Maximum	Unit
Vo	Output voltage	2.4	2.5	3.1	V

Symbol	Description	Minimum	Typical	Maximum	Unit
Io	Output current	–	–	100	mA
Co	External decoupling capacitor	–	1	–	uF

4.3.2. LDO18

The built–in LDO18 is used for power supply of PSRAM IO and PSRAM. Voltage is configurable. Its electrical characteristics are as follows:

Symbol	Description	Minimum	Typical	Maximum	Unit
Vo	Output voltage	1.71	1.8	1.92	V
Io	Output current	–	–	100	mA
Co	External decoupling capacitor	–	1	–	uF

4.3.3. LDO1x

The built–in LDO1x is used for power supply of VDD11_SYS. Voltage is configurable. Its electrical characteristics are as follows:

Symbol	Description	Minimum	Typical	Maximum	Unit
Vo	Output voltage	1.0	1.1	1.375	V
Io	Output current	–	–	200	mA
Co	External decoupling capacitor	–	1	–	uF

4.4. IO Electrical Features

4.4.1. IO DC Electrical Features

Symbol	Description	Minimum	Typical	Maximum	Unit
VIH	High–level input voltage	0.7 * VCC33_IO	–	VCC33_IO + 0.3	V
VIL	Low–level input voltage	–0.3	–	0.3 * VCC33_IO	V
RPU	Pullup resistor	–	33	–	KΩ
RPD	Pulldown resistor	–	33	–	KΩ
IIH	High–level input current	–	–	10	uA
IIL	Low–level input current	–	–	10	uA
VOH	High–level output voltage	VCC33_IO + 0.3	–	For VCC33_IO	V
VOL	Low–level output voltage	0	–	0.3	V
IOH	High–level output current	8	–	60	mA
IOL	Low–level output current	8	–	55	mA
IOZ	Tri–stated output leakage current	–10	–	10	uA
CIN	Input capacitance	–	–	5	pF
COUT	Output capacitance	–	–	5	pF

4.4.2. IO AC Electrical Features

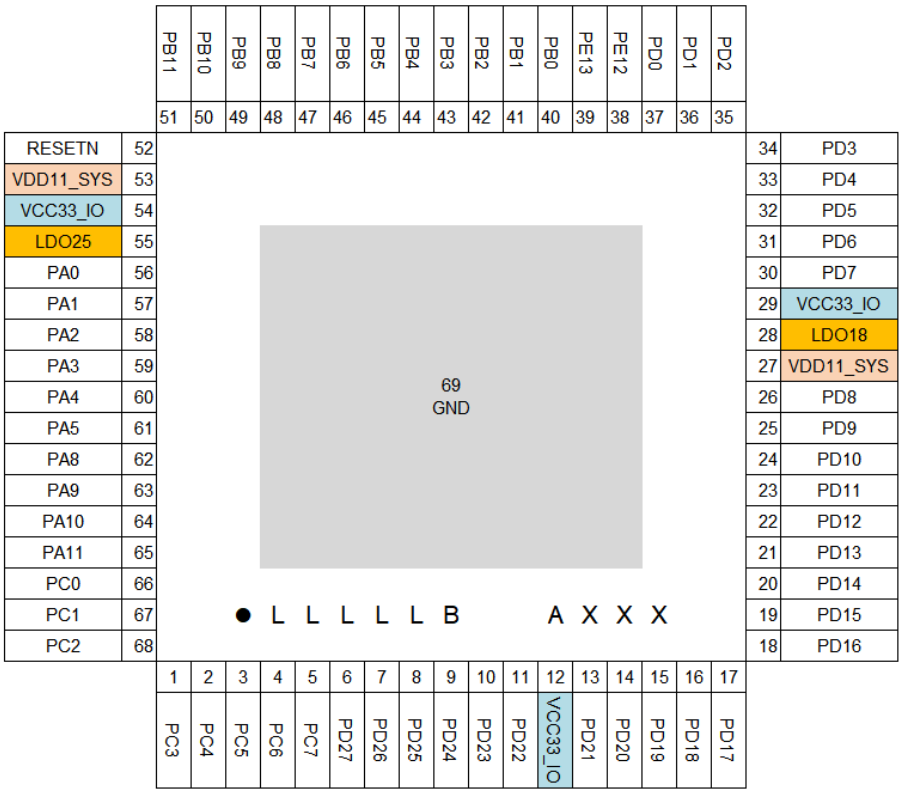
Symbol	Description	Test Conditions	Minimum	Typical	Maximum	Unit
fmax	Maximum frequency	6pF of load capacitance	–	–	150	MHz
TR230	Rise time	Time between VOL and VOH	–	–	1.6	ns

Symbol	Description	Test Conditions	Minimum	Typical	Maximum	Unit
tf	Fall time	Time between VOH and VOL	–	–	1.6	ns

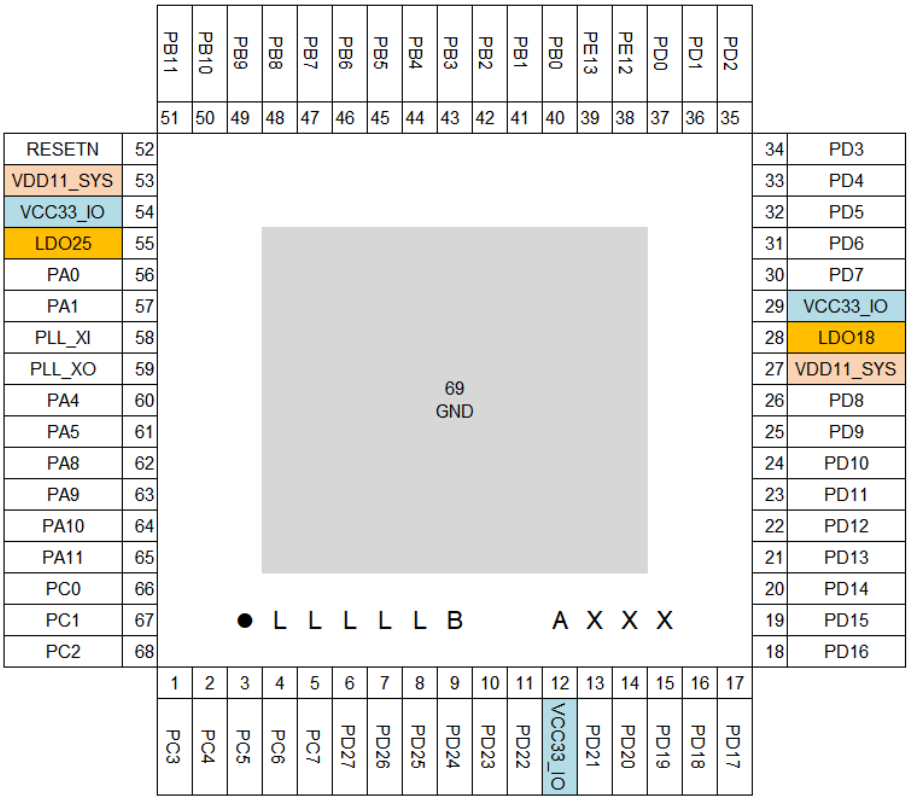
5. Package Information

5.1. Pin Distribution

5.1.1. D121 QFN68



5.1.2. D123 QFN68



LLLLLB: LLLLL indicates bacth number, and B is a fixed letter.

AXXX: XXX indictaes date code, and A is a fixed letter.

5.2. Pin Attributes

Note:

- [1]: Serial number of pin in the package
- [2]: Name of pin in the package
- [3]: Signal Type, to indicate signal directions
  - I – Input
  - O – Output
  - I/O – Input/ Output
  - A – Analog
  - AI – Analog Input
  - AO – Analog Output
  - P – Power
  - G – Ground
- [4]: Pin reset status, PU means pullup, PD means pulldown, and Z means high impedance state.
- [5]: PU/PD means there are internal pullup and pulldown resistors which can be enable and disable by software.

- [6]: Default output current. For GPIO, the default output current is 20 mA and the maximum is 50 mA.
- [7]: Power source

Table 5–1 D121 Pin Attribute

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA)[6]	Power Source[7]
GPIO A						
56	PA0	I/O	Z	PU/PD	20	For VCC33_IO
57	PA1	I/O	Z	PU/PD	20	For VCC33_IO
58	PA2	I/O	Z	PU/PD	20	For VCC33_IO
59	PA3	I/O	Z	PU/PD	20	For VCC33_IO
60	PA4	I/O	Z	PU/PD	20	For VCC33_IO
61	PA5	I/O	Z	PU/PD	20	For VCC33_IO
62	PA8	I/O	Z	PU/PD	20	For VCC33_IO
63	PA9	I/O	Z	PU/PD	20	For VCC33_IO
64	PA10	I/O	PU	PU/PD	20	For VCC33_IO
65	PA11	I/O	PU	PU/PD	20	For VCC33_IO
GPIO B						
40	PB0	I/O	Z	PU/PD	20	For VCC33_IO
41	PB1	I/O	Z	PU/PD	20	For VCC33_IO
42	PB2	I/O	Z	PU/PD	20	For VCC33_IO
43	PB3	I/O	Z	PU/PD	20	For VCC33_IO
44	PB4	I/O	Z	PU/PD	20	For VCC33_IO
45	PB5	I/O	Z	PU/PD	20	For VCC33_IO
46	PB6	I/O	Z	PU/PD	20	For VCC33_IO
47	PB7	I/O	Z	PU/PD	20	For VCC33_IO
48	PB8	I/O	Z	PU/PD	20	For VCC33_IO
49	PB9	I/O	Z	PU/PD	20	For VCC33_IO
50	PB10	I/O	Z	PU/PD	20	For VCC33_IO
51	PB11	I/O	Z	PU/PD	20	For VCC33_IO
GPIO C						
66	PC0	I/O	Z	PU/PD	20	For VCC33_IO
67	PC1	I/O	Z	PU/PD	20	For VCC33_IO
68	PC2	I/O	Z	PU/PD	20	For VCC33_IO
1	PC3	I/O	Z	PU/PD	20	For VCC33_IO
2	PC4	I/O	Z	PU/PD	20	For VCC33_IO
3	PC5	I/O	Z	PU/PD	20	For VCC33_IO
4	PC6	I/O	Z	PU/PD	20	For VCC33_IO
5	PC7	I/O	Z	PU/PD	20	For VCC33_IO
GPIO D						
37	PD0	I/O	Z	PU/PD	20	For VCC33_IO
36	PD1	I/O	Z	PU/PD	20	For VCC33_IO

Table 5–1 D121 Pin Attribute (continued)

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA)[6]	Power Source[7]
35	PD2	I/O	Z	PU/PD	20	For VCC33_IO
34	PD3	I/O	Z	PU/PD	20	For VCC33_IO
33	PD4	I/O	Z	PU/PD	20	For VCC33_IO
32	PD5	I/O	Z	PU/PD	20	For VCC33_IO
31	PD6	I/O	Z	PU/PD	20	For VCC33_IO
30	PD7	I/O	Z	PU/PD	20	For VCC33_IO
26	PD8	I/O	Z	PU/PD	20	For VCC33_IO
25	PD9	I/O	Z	PU/PD	20	For VCC33_IO
24	PD10	I/O	Z	PU/PD	20	For VCC33_IO
23	PD11	I/O	Z	PU/PD	20	For VCC33_IO
22	PD12	I/O	Z	PU/PD	20	For VCC33_IO
21	PD13	I/O	Z	PU/PD	20	For VCC33_IO
20	PD14	I/O	Z	PU/PD	20	For VCC33_IO
19	PD15	I/O	Z	PU/PD	20	For VCC33_IO
18	PD16	I/O	Z	PU/PD	20	For VCC33_IO
17	PD17	I/O	Z	PU/PD	20	For VCC33_IO
16	PD18	I/O	Z	PU/PD	20	For VCC33_IO
15	PD19	I/O	Z	PU/PD	20	For VCC33_IO
14	PD20	I/O	Z	PU/PD	20	For VCC33_IO
13	PD21	I/O	Z	PU/PD	20	For VCC33_IO
11	PD22	I/O	Z	PU/PD	20	For VCC33_IO
10	PD23	I/O	Z	PU/PD	20	For VCC33_IO
9	PD24	I/O	Z	PU/PD	20	For VCC33_IO
8	PD25	I/O	Z	PU/PD	20	For VCC33_IO
7	PD26	I/O	Z	PU/PD	20	For VCC33_IO
6	PD27	I/O	Z	PU/PD	20	For VCC33_IO
GPIO E						
38	PE12	I/O	Z	PU/PD	20	LDO25
39	PE13	I/O	Z	PU/PD	20	LDO25
PLL						
52	RESETN	I	–	–	–	–
Power						
12, 29, 54	For VCC33_IO	P	–	–	–	–
55	LDO25	P	–	–	–	–
28	LDO18	P	–	–	–	–
27, 53	VDD11_SYS	P	–	–	–	–

Table 5–1 D121 Pin Attribute (continued)

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA)[6]	Power Source[7]
69	GND	P	–	–	–	–

Table 5–2 D123 Pin Attribute

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA)[6]	Power Source[7]
GPIO A						
56	PA0	I/O	Z	PU/PD	20	For VCC33_IO
57	PA1	I/O	Z	PU/PD	20	For VCC33_IO
58	PLL_XI	I	–	–	–	–
59	PLL_XO	O	–	–	–	–
60	PA4	I/O	Z	PU/PD	20	For VCC33_IO
61	PA5	I/O	Z	PU/PD	20	For VCC33_IO
62	PA8	I/O	Z	PU/PD	20	For VCC33_IO
63	PA9	I/O	Z	PU/PD	20	For VCC33_IO
64	PA10	I/O	PU	PU/PD	20	For VCC33_IO
65	PA11	I/O	PU	PU/PD	20	For VCC33_IO
GPIO B						
40	PB0	I/O	Z	PU/PD	20	For VCC33_IO
41	PB1	I/O	Z	PU/PD	20	For VCC33_IO
42	PB2	I/O	Z	PU/PD	20	For VCC33_IO
43	PB3	I/O	Z	PU/PD	20	For VCC33_IO
44	PB4	I/O	Z	PU/PD	20	For VCC33_IO
45	PB5	I/O	Z	PU/PD	20	For VCC33_IO
46	PB6	I/O	Z	PU/PD	20	For VCC33_IO
47	PB7	I/O	Z	PU/PD	20	For VCC33_IO
48	PB8	I/O	Z	PU/PD	20	For VCC33_IO
49	PB9	I/O	Z	PU/PD	20	For VCC33_IO
50	PB10	I/O	Z	PU/PD	20	For VCC33_IO
51	PB11	I/O	Z	PU/PD	20	For VCC33_IO
GPIO C						
66	PC0	I/O	Z	PU/PD	20	For VCC33_IO
67	PC1	I/O	Z	PU/PD	20	For VCC33_IO
68	PC2	I/O	Z	PU/PD	20	For VCC33_IO
1	PC3	I/O	Z	PU/PD	20	For VCC33_IO
2	PC4	I/O	Z	PU/PD	20	For VCC33_IO
3	PC5	I/O	Z	PU/PD	20	For VCC33_IO
4	PC6	I/O	Z	PU/PD	20	For VCC33_IO
5	PC7	I/O	Z	PU/PD	20	For VCC33_IO
GPIO D						
37	PD0	I/O	Z	PU/PD	20	For VCC33_IO
36	PD1	I/O	Z	PU/PD	20	For VCC33_IO

Table 5–2 D123 Pin Attribute (continued)

Pins [1]	Name [2]	Signal Type [3]	Reset Status[4]	Pullup and Pulldown [5]	Default output current (mA)[6]	Power Source[7]
35	PD2	I/O	Z	PU/PD	20	For VCC33_IO
34	PD3	I/O	Z	PU/PD	20	For VCC33_IO
33	PD4	I/O	Z	PU/PD	20	For VCC33_IO
32	PD5	I/O	Z	PU/PD	20	For VCC33_IO
31	PD6	I/O	Z	PU/PD	20	For VCC33_IO
30	PD7	I/O	Z	PU/PD	20	For VCC33_IO
26	PD8	I/O	Z	PU/PD	20	For VCC33_IO
25	PD9	I/O	Z	PU/PD	20	For VCC33_IO
24	PD10	I/O	Z	PU/PD	20	For VCC33_IO
23	PD11	I/O	Z	PU/PD	20	For VCC33_IO
22	PD12	I/O	Z	PU/PD	20	For VCC33_IO
21	PD13	I/O	Z	PU/PD	20	For VCC33_IO
20	PD14	I/O	Z	PU/PD	20	For VCC33_IO
19	PD15	I/O	Z	PU/PD	20	For VCC33_IO
18	PD16	I/O	Z	PU/PD	20	For VCC33_IO
17	PD17	I/O	Z	PU/PD	20	For VCC33_IO
16	PD18	I/O	Z	PU/PD	20	For VCC33_IO
15	PD19	I/O	Z	PU/PD	20	For VCC33_IO
14	PD20	I/O	Z	PU/PD	20	For VCC33_IO
13	PD21	I/O	Z	PU/PD	20	For VCC33_IO
11	PD22	I/O	Z	PU/PD	20	For VCC33_IO
10	PD23	I/O	Z	PU/PD	20	For VCC33_IO
9	PD24	I/O	Z	PU/PD	20	For VCC33_IO
8	PD25	I/O	Z	PU/PD	20	For VCC33_IO
7	PD26	I/O	Z	PU/PD	20	For VCC33_IO
6	PD27	I/O	Z	PU/PD	20	For VCC33_IO
GPIO E						
38	PE12	I/O	Z	PU/PD	20	LDO25
39	PE13	I/O	Z	PU/PD	20	LDO25
PLL						
52	RESETN	I	–	–	–	–
Power						
12, 29, 54	For VCC33_IO	P	–	–	–	–
55	LDO25	P	–	–	–	–
28	LDO18	P	–	–	–	–
27, 53	VDD11_SYS	P	–	–	–	–
69	GND	P	–	–	–	–

5.3. Pin–Mux

5.3.1. D12x Pin–mux

Table 5–3 D12x Pin–mux

Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 8
PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX	–	CPU_NMI
PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX	–	DE_TE
PA2	GPADC2	CAN1_TX	I2C1_SCL	UART1_TX	–	UART2_CTS
PA3	GPADC3	CAN1_RX	I2C1_SDA	UART1_RX	–	UART2_RTS
PA4	GPADC4	–	CAN0_TX	UART2_TX	–	–
PA5	GPADC5	–	CAN0_RX	UART2_RX	–	–
PA8	RTP_XP	–	I2C0_SCL	–	–	–
PA9	RTP_YP	–	I2C0_SDA	–	–	–
PA10	RTP_XN	IR_RX	–	–	–	JTAG_MS
PA11	RTP_YN	IR_TX	–	–	–	JTAG_CK
PB0	SPI0_WP	SPI1_WP	–	UART0_TX	–	–
PB1	SPI0_MISO	SPI1_MISO	–	UART2_TX	–	–
PB2	SPI0_CS0	SPI1_CS0	–	UART2_RX	–	–
PB3	SPI0_HOLD	SPI1_HOLD	–	UART0_RX	–	–
PB4	SPI0_CLK	SPI1_CLK	–	UART2_RTS	–	–
PB5	SPI0_MOSI	SPI1_MOSI	–	UART0_RTS	UART2_CTS	–
PB6	SDC0_CMD	SPI1_CS0	–	UART1_TX	–	–
PB7	SDC0_CLK	SPI1_MISO	–	UART1_RX	–	–
PB8	SDC0_D3	SPI1_MOSI	–	UART1_RTS	UART3_CTS	–
PB9	SDC0_D0	SPI1_CLK	–	UART3_RTS	–	–
PB10	SDC0_D1	SPI1_HOLD	–	UART3_TX	–	–
PB11	SDC0_D2	SPI1_WP	–	UART3_RX	–	–
PC0	SDC1_D1	–	I2C0_SCL	UART3_RTS	–	JTAG_MS
PC1	SDC1_D0	–	–	–	–	–
PC2	SDC1_CLK	–	–	–	–	UART0_TX
PC3	SDC1_CMD	–	–	–	–	–
PC4	SDC1_D3	PWM0_A	I2C1_SCL	UART3_TX	–	UART0_RX
PC5	SDC1_D2	PWM0_B	I2C1_SDA	UART3_RX	–	JTAG_CK
PC6	SDC1_DET	PWM1_A	I2C0_SDA	UART3_CTS	DE_TE	IR_RX
PC7	–	PWM1_B	–	–	–	IR_TX
PD0	LCD_D0	CAN0_TX	I2C0_SCL	UART0_TX	–	–
PD1	LCD_D1	CAN0_RX	I2C0_SDA	UART0_RX	–	–
PD2	LCD_D2	CAN1_TX	I2C1_SCL	UART1_TX	–	–
PD3	LCD_D3	CAN1_RX	I2C1_SDA	UART1_RX	–	–
PD4	LCD_D4	–	I2C1_SCL	UART2_TX	–	–
PD5	LCD_D5	–	I2C1_SDA	UART2_RX	–	–
PD6	LCD_D6	–	PWM0_A	DSPK0	–	–
PD7	LCD_D7	–	PWM0_B	DSPK1	–	–

Table 5–3 D12x Pin–mux (continued)

Pins	Function 2	Function 3	Function 4	Function 5	Function 6	Function 8
PD8	LCD_D8	–	PWM1_A	–	–	–
PD9	LCD_D9	–	–	–	–	–
PD10	LCD_D10	–	–	–	–	–
PD11	LCD_D11	–	–	–	–	–
PD12	LCD_D12	–	–	–	–	–
PD13	LCD_D13	–	–	–	–	–
PD14	LCD_D14	–	–	–	–	–
PD15	LCD_D15	–	–	–	–	–
PD16	LCD_D16	–	–	–	–	–
PD17	LCD_D17	–	–	–	–	–
PD18	LCD_D18	–	–	–	–	–
PD19	LCD_D19	–	–	–	–	–
PD20	LCD_D20	–	–	–	–	–
PD21	LCD_D21	–	–	–	–	–
PD22	LCD_D22	–	–	–	–	–
PD23	LCD_D23	–	–	–	–	–
PD24	LCD_DCLK	–	–	–	–	–
PD25	LCD_HS	–	–	–	PWM0_B	–
PD26	LCD_VS	–	–	–	PWM1_A	–
PD27	LCD_DE	–	–	–	PWM1_B	–
PE12	–	PWM1_B	–	DSPK1	–	–
PE13	–	PWM0_A	–	DSPK0	–	–

5.3.2. D12x QFN68 Package Pin Description

Table 5–4 D12x QFN68 Package Pin Description

Pins	Definition	Signal Type	Function	Remark
SYSTEM				
52	RESETN	INPUT	System Reset	Built in with a 30kΩ pullup resistor and dithering filter which can be floating if not used. If an external capacitor is connected, the recommended load capacitance is less than 4.7 uF.
POWER				
12, 29, 54	For VCC33_IO	POWER	IO Voltage	3.3 –V power supply
55	LDO25	POWER	Built–in LDO output	Used for internal analog modules, and connected with a 1–uF bypass capacitor
28	LDO18	POWER	Built–in LDO output	Used for internal PSRAM modules. If used otherwise, chip cooling must be considered. Connect with a 1–uF bypass capacitor
27, 53	VDD11_SYS	POWER	Chip Core Voltage	1.1 V power supply. If the built–in LDO1x is used, chip cooling must be considered. Pin 53 is LDO1x output.
69	GND	POWER	–	GND Copper full–cover connection via stitching for cooling.

5.3.3. D121 QFN68 Package Pin–mux

Table 5–5 D121 QFN68 Package Pin–mux

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 8
GPIO A							
56	PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX	–	CPU_NMI
57	PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX	–	DE_TE
58	PA2	GPADC2	–	I2C1_SCL	UART1_TX	–	
59	PA3	GPADC3	–	I2C1_SDA	UART1_RX	–	
60	PA4	GPADC4	–	–	UART2_TX	–	–
61	PA5	GPADC5	–	–	UART2_RX	–	–
62	PA8	RTP_XP	–	I2C0_SCL	–	–	–
63	PA9	RTP_YP	–	I2C0_SDA	–	–	–
64	PA10	RTP_XN	IR_RX	–	–	–	JTAG_MS
65	PA11	RTP_YN	IR_TX	–	–	–	JTAG_CK
GPIO B							
40	PB0	SPI0_WP	SPI1_WP	–	UART0_TX	–	–
41	PB1	SPI0_MISO	SPI1_MISO	–	UART2_TX	–	–
42	PB2	SPI0_CS0	SPI1_CS0	–	UART2_RX	–	–
43	PB3	SPI0_HOLD	SPI1_HOLD	–	UART0_RX	–	–
44	PB4	SPI0_CLK	SPI1_CLK	–	UART2_RTS	–	–
45	PB5	SPI0_MOSI	SPI1_MOSI	–	UART0_RTS	UART2_CTS	–
46	PB6	SDC0_CMD	SPI1_CS0	–	UART1_TX	–	–
47	PB7	SDC0_CLK	SPI1_MISO	–	UART1_RX	–	–
48	PB8	SDC0_D3	SPI1_MOSI	–	UART1_RTS	UART3_CTS	–
49	PB9	SDC0_D0	SPI1_CLK	–	UART3_RTS	–	–
50	PB10	SDC0_D1	SPI1_HOLD	–	UART3_TX	–	–
51	PB11	SDC0_D2	SPI1_WP	–	UART3_RX	–	–
GPIO C							
66	PC0	SDC1_D1	–	I2C0_SCL	UART3_RTS	–	JTAG_MS
67	PC1	SDC1_D0	–	–	–	–	–
68	PC2	SDC1_CLK	–	–	–	–	UART0_TX
1	PC3	SDC1_CMD	–	–	–	–	–
2	PC4	SDC1_D3	PWM0_A	I2C1_SCL	UART3_TX	–	UART0_RX
3	PC5	SDC1_D2	PWM0_B	I2C1_SDA	UART3_RX	–	JTAG_CK
4	PC6	SDC1_DET	PWM1_A	I2C0_SDA	UART3_CTS	DE_TE	IR_RX
5	PC7	–	PWM1_B	–	–	–	IR_TX
GPIO D							
37	PD0	LCD_D0	–	I2C0_SCL	UART0_TX	–	–
36	PD1	LCD_D1	–	I2C0_SDA	UART0_RX	–	–
35	PD2	LCD_D2	–	I2C1_SCL	UART1_TX	–	–
34	PD3	LCD_D3	–	I2C1_SDA	UART1_RX	–	–
33	PD4	LCD_D4	–	I2C1_SCL	UART2_TX	–	–

Table 5–5 D121 QFN68 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 8
32	PD5	LCD_D5	–	I2C1_SDA	UART2_RX	–	–
31	PD6	LCD_D6	–	PWM0_A	DSPK0	–	–
30	PD7	LCD_D7	–	PWM0_B	DSPK1	–	–
26	PD8	LCD_D8	–	PWM1_A	–	–	–
25	PD9	LCD_D9	–	–	–	–	–
24	PD10	LCD_D10	–	–	–	–	–
23	PD11	LCD_D11	–	–	–	–	–
22	PD12	LCD_D12	–	–	–	–	–
21	PD13	LCD_D13	–	–	–	–	–
20	PD14	LCD_D14	–	–	–	–	–
19	PD15	LCD_D15	–	–	–	–	–
18	PD16	LCD_D16	–	–	–	–	–
17	PD17	LCD_D17	–	–	–	–	–
16	PD18	LCD_D18	–	–	–	–	–
15	PD19	LCD_D19	–	–	–	–	–
14	PD20	LCD_D20	–	–	–	–	–
13	PD21	LCD_D21	–	–	–	–	–
11	PD22	LCD_D22	–	–	–	–	–
10	PD23	LCD_D23	–	–	–	–	–
9	PD24	LCD_DCLK	–	–	–	–	–
8	PD25	LCD_HS	–	–	–	PWM0_B	–
7	PD26	LCD_VS	–	–	–	PWM1_A	–
6	PD27	LCD_DE	–	–	–	PWM1_B	–
GPIO E							
38	PE12	–	PWM1_B	–	DSPK1	–	–
39	PE13	–	PWM0_A	–	DSPK0	–	–

5.3.4. D123 QFN68 Package Pin–mux

Table 5–6 D123 QFN68 Package Pin–mux

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 8
GPIO A							
56	PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX	–	CPU_NMI
57	PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX	–	DE_TE
58	PLL_XI	–	–	–	–	–	–
59	PLL_XO	–	–	–	–	–	–
60	PA4	GPADC4	–	CAN0_TX	UART2_TX	–	–
61	PA5	GPADC5	–	CAN0_RX	UART2_RX	–	–
62	PA8	RTP_XP	–	I2C0_SCL	–	–	–
63	PA9	RTP_YP	–	I2C0_SDA	–	–	–
64	PA10	RTP_XN	IR_RX	–	–	–	JTAG_MS
65	PA11	RTP_YN	IR_TX	–	–	–	JTAG_CK

Table 5–6 D123 QFN68 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 8
GPIO B							
40	PB0	SPI0_WP	SPI1_WP	–	UART0_TX	–	–
41	PB1	SPI0_MISO	SPI1_MISO	–	UART2_TX	–	–
42	PB2	SPI0_CS0	SPI1_CS0	–	UART2_RX	–	–
43	PB3	SPI0_HOLD	SPI1_HOLD	–	UART0_RX	–	–
44	PB4	SPI0_CLK	SPI1_CLK	–	UART2_RTS	–	–
45	PB5	SPI0_MOSI	SPI1_MOSI	–	UART0_RTS	UART2_CTS	–
46	PB6	SDC0_CMD	SPI1_CS0	–	UART1_TX	–	–
47	PB7	SDC0_CLK	SPI1_MISO	–	UART1_RX	–	–
48	PB8	SDC0_D3	SPI1_MOSI	–	UART1_RTS	UART3_CTS	–
49	PB9	SDC0_D0	SPI1_CLK	–	UART3_RTS	–	–
50	PB10	SDC0_D1	SPI1_HOLD	–	UART3_TX	–	–
51	PB11	SDC0_D2	SPI1_WP	–	UART3_RX	–	–
GPIO C							
66	PC0	SDC1_D1	–	I2C0_SCL	UART3_RTS	–	JTAG_MS
67	PC1	SDC1_D0	–	–	–	–	–
68	PC2	SDC1_CLK	–	–	–	–	UART0_TX
1	PC3	SDC1_CMD	–	–	–	–	–
2	PC4	SDC1_D3	PWM0_A	I2C1_SCL	UART3_TX	–	UART0_RX
3	PC5	SDC1_D2	PWM0_B	I2C1_SDA	UART3_RX	–	JTAG_CK
4	PC6	SDC1_DET	PWM1_A	I2C0_SDA	UART3_CTS	DE_TE	IR_RX
5	PC7	–	PWM1_B	–	–	–	IR_TX
GPIO D							
37	PD0	LCD_D0	CAN0_TX	I2C0_SCL	UART0_TX	–	–
36	PD1	LCD_D1	CAN0_RX	I2C0_SDA	UART0_RX	–	–
35	PD2	LCD_D2	CAN1_TX	I2C1_SCL	UART1_TX	–	–
34	PD3	LCD_D3	CAN1_RX	I2C1_SDA	UART1_RX	–	–
33	PD4	LCD_D4	–	I2C1_SCL	UART2_TX	–	–
32	PD5	LCD_D5	–	I2C1_SDA	UART2_RX	–	–
31	PD6	LCD_D6	–	PWM0_A	DSPK0	–	–
30	PD7	LCD_D7	–	PWM0_B	DSPK1	–	–
26	PD8	LCD_D8	–	PWM1_A	–	–	–
25	PD9	LCD_D9	–	–	–	–	–
24	PD10	LCD_D10	–	–	–	–	–
23	PD11	LCD_D11	–	–	–	–	–
22	PD12	LCD_D12	–	–	–	–	–
21	PD13	LCD_D13	–	–	–	–	–
20	PD14	LCD_D14	–	–	–	–	–
19	PD15	LCD_D15	–	–	–	–	–
18	PD16	LCD_D16	–	–	–	–	–
17	PD17	LCD_D17	–	–	–	–	–

Table 5–6 D123 QFN68 Package Pin–mux (continued)

Pins	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 8
16	PD18	LCD_D18	–	–	–	–	–
15	PD19	LCD_D19	–	–	–	–	–
14	PD20	LCD_D20	–	–	–	–	–
13	PD21	LCD_D21	–	–	–	–	–
11	PD22	LCD_D22	–	–	–	–	–
10	PD23	LCD_D23	–	–	–	–	–
9	PD24	LCD_DCLK	–	–	–	–	–
8	PD25	LCD_HS	–	–	–	PWM0_B	–
7	PD26	LCD_VS	–	–	–	PWM1_A	–
6	PD27	LCD_DE	–	–	–	PWM1_B	–
GPIO E							
38	PE12	–	PWM1_B	–	DSPK1	–	–
39	PE13	–	PWM0_A	–	DSPK0	–	–

5.4. Pin Description

Pin/Signal Name	Description	Signal Type
SYSTEM		
RESETN	Reset pin	I
PLL_XI	24M crystal oscillator input capacitance	I
PLL_XO	24M crystal oscillator output capacitance	O
RTP		
RTP_XP	RTP X positive, which can be used for ADC functions if RTP is not used	AI
RTP_YP	RTP Y positive, which can be used for ADC functions if RTP is not used	AI
RTP_XN	RTP X negative, which can be used for ADC functions if RTP is not used	AI
RTP_YN	RTP Y negative, which can be used for ADC functions if RTP is not used	AI
ADC, x = 0~5		
GPADCx	General–purpose analog input	AI
PWM，x = 0~1		
PWMx_A	PWMx Channel A	O
PWMx_B	PWMx Channel B	O
QSPI, x = 0~1		
SPIx_HOLD	SPIx hold signal, valid for low–level voltage	I/O
SPIx_WP	SPIx write protection, valid for low–level voltage	I/O
SPIx_CS	SPIx chip select signal, valid for low–level voltage.	I/O
SPIx_CLK	SPIx clock signal	I/O
SPIx_MOSI	SPIx master out slave in	I/O
SPIx_MISO	SPIx master in slave out	I/O
UART，x = 0~3		
UARTx_TX	UARTx data transmission	O
UARTx_RX	UARTx data reception	I

Pin/Signal Name	Description	Signal Type
UARTx_CTS	UARTx confirmed transmission	I
UARTx_RTS	UARTx requested transmission	O
I2C，x = 0~1		
I2Cx_SCL	I2C serial clock line	I/O
I2Cx_SDA	I2Cx serial data line	I/O
CAN		
CAN0_TX	CAN0 data transmission, connected with a CAN transceiver	O
CAN0_RX	CAN0 data reception, connected with a CAN receiver	I
CAN1_TX	CAN1 data t, connected with a CAN receiver	O
CAN1_RX	CAN1 data reception, connected with a CAN receiver	I
CIR		
IR_TX	Infrared data transmit	O
IR_RX	Infrared data receive	I
DSPK		
DSPK0	Speaker signal output channel 0	O
DSPK1	Speaker signal output channel 1	O
SDC, x = 0~1		
SDCx_CMD	SDC0 command signal	I/O
SDCx_CLK	SDC0 clock signal	O
SDCx_D[3:0]	SDC0 data output/input	I/O
LCD		
LCD_D[23:0]	LCD data output	O
LCD_DCLK	LCD clock data signal	O
LCD_HS	LCD horizontal synchronization	O
LCD_VS	LCD vertical synchronization	O
LCD_DE	LCD data enable	O

5.5. Package Size

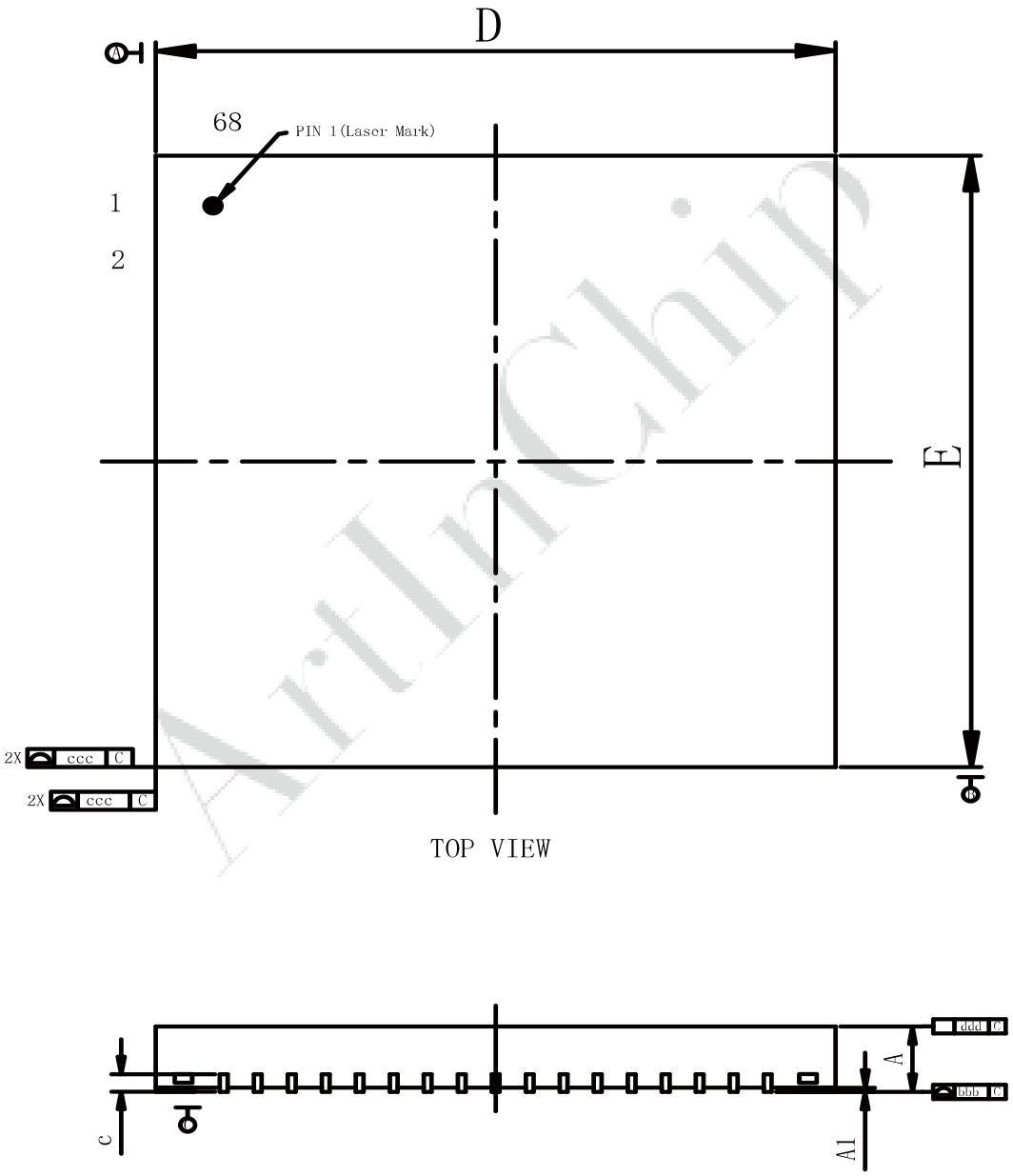
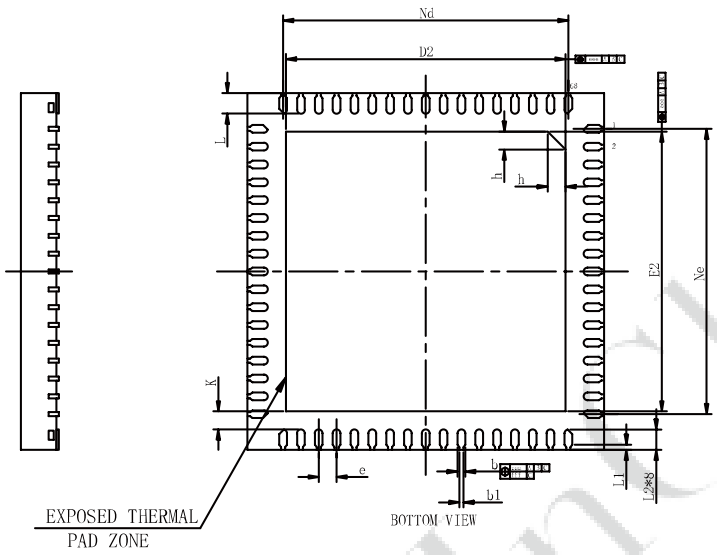


Figure 5–1 QFN68 Packaging TOP



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.80	0.85	0.90	
A1	—	0.02	0.05	
b	0.10	0.15	0.20	
b1	0.08REF			
c	0.18	0.20	0.25	
D	6.90	7.00	7.10	
D2	5.39	5.49	5.59	
e	0.35BSC			
Nd	5.60BSC			
E	6.90	7.00	7.10	
E2	5.39	5.49	5.59	
Ne	5.60BSC			
L	0.35	0.40	0.45	
L1	0.10REF			
L2	0.30	0.40	0.50	⚠
K	0.20	--	--	
h	0.30	0.35	0.40	
aaa	0.07			
bbb	0.08			
ccc	0.10			
ddd	0.10			
eee	0.10			
fff	0.05			

Figure 5–2 QFN68 Packaging BOTTOM